Technical Report
RAL-TR-96-041

Report of the EPSRC Parallel Processing in Engineering Community Club (PPECC)

C P Wadsworth and B W Henderson

June 1996

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ISSN 1358-6254

REPORT
OF THE EPSRC
PARALLEL PROCESSING IN ENGINEERING
COMMUNITY CLUB
(PPECC)

May 1993 - March 1996

C P Wadsworth and B W Henderson

March 1996

Parallel and Distributed Systems Group
Computing and Information Systems Department
Rutherford Appleton Laboratory
Chilton, Didcot
Oxon OX11 0QX

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APPENDICES

Summary

The Parallel Processing in Engineering Community Club (PPECC) was founded in May 1993 as one of the three Community Clubs setup by the Engineering and Physical Sciences Research Council (EPSRC). The report covers the period May 1993 to March 1996 during which PPECC has grown and developed. The membership of the Club reflects the diversity of applications and research activities in which parallel computing techniques have made an impact, from the development of new compiler technology to the parallelisation of engineering design software.

The main achievements of PPECC since its foundation are summarised below:

- **Technical Meetings:** PPECC has organised four technical meetings and workshops. The subjects of these meetings again reflect the diversity of the Club's membership. In general these meetings have been well attended and the level of contributions and discussion has been excellent.;
- **Courses on Parallel Processing:** A popular feature of PPECC has been the courses on parallel computing. These have always been heavily subscribed; in particular the course on 'Parallel Processing Techniques'. Four of these two-days course were organised during this period;
- **Parallel Evaluation Centre (PEC):** The Parallel Evaluation Centre was set up to allow members to perform their own evaluation of current parallel processing hardware. The PEC built up a collection of 'low-cost' parallel hardware that could be added to PC and workstation configurations. Usage of these systems has been limited by the lack of good networking software which has required members coming to the centre to perform their evaluations;
- **Mailshots, Publicity and Liaison:** PPECC has continued over the years to provide its members with information on parallel processing events and hardware. This has been achieved using the Engineering Computing Newsletter (ECN), mailbase, e-mail and the World Wide Web.

With the change in emphasis in parallel and distributed computing towards techniques such as domain decomposition and away from the hardware technology the future of PPECC is seen to be in promoting these advanced computing techniques required to exploit the available hardware systems. This change of direction also enables PPECC to widen its view on the world. As a result of this perceived change in the requirements of the research community, the PPECC Steering Group has thought it timely and appropriate to change the name of PPECC to the Advanced Computing Techniques Community Club - ACTCC.

EPSRC has agreed with this change and have supported the Steering Group's decision. As a result the next event being planned by the Steering Group is the "re-launch" of the PPECC as ACTCC.

PPECC: 1993-96 Highlights

Membership

- **grown from 0 (May 93) to 193 (April 94) to 271 (March 96)**

Steering Group

- Chairman: Brian Hoyle (Leeds)
- expanded to 6 community members (1 industrial)
- 5 meetings (Apr 94, Jul 94, Dec 94, May 95, Feb 96)

Inaugural Meeting/Seminar

- RAL, 1 June 94; 7 speakers, 55 attendees (booklet)

Seminars

- "*Embedded Parallel Processing*" (booklet)
- "*Parallel Field Analysis in Engineering*", RAL, 11 July 95 (booklet)

Workshop

- "*Distributed vs Parallel: convergence or divergence?*", 14-15 March 95
- 7 invited speakers, 19 position papers, 44 attendees
- separate report available

Courses

- "*Parallel Fortran for Engineers*", 13-14 July 94 & 14-15 June 95
- "*Parallel Processing Techniques*", 25-26 Oct 94
- "*Parallel C for Engineers*", 18-19 Jan 95

Parallel Evaluation Centre (PEC)

- people: advice etc
- kit: range of i860, C40, transputer, Sparc10 and multi-processor PC systems

Liaison

- with BCS PPSG: Treasurer; "*Programming with Threads*", 18 Dec 95
- UKPAR'96 Programme Committee and EUROPAR'96 Advisory Board: member
- EPSRC Portable Software Tools for Parallel Architectures (PSTPA): Coordinator

Mailshots and Publicity

- Mailshot to members, Aug 94 (by email reflector since)
- PPECC and PEC brochures produced and distributed
- 2-monthly ECN page + 5 special articles
- email reflector at ppecc@mailbase.ac.uk
- WWW server at http://www.cis.rl.ac.uk/clubs/PPECC/index.html

1. INTRODUCTION

This report covers the activities of the Parallel Processing in Engineering Community Club (PPECC) since the announcement of its formation in May 1993.

The report is structured like a hypertext document. The main body in Sections 1-6 provides a broad overview which also points to more detailed material in Appendices. The Appendices are numbered to correspond to the Sections in the main body, i.e. Appendix 4.1.1a is the first Appendix referenced in Section 4.1.1, Appendix 4.1.1b is the second, and so on. Lengthier material is not included here but is available separately from the PPECC support staff at RAL. A list may be found in Appendix 1a.

Sections 2 and 3 cover the background to the Club, the profile of its membership, and the role of the Steering Group. Section 4 presents an account of activities during the period and is the heart of the report. Future plans are outlined in Section 5. Finally, Section 6 tells you where to find yet more information or get help with technical or other enquiries.

2. BACKGROUND AND OBJECTIVES

PPECC has been formed following the successful examples for two other areas (CFD, Visualisation) of the EASE Programme, initially under the auspices of the Engineering Research Commission of SERC, latterly under the Core Engineering Programmes sector of EPSRC since April 1994.

The motivation for a Club in parallel processing stemmed from the increasing number of engineering researchers proposing to use parallel processing techniques. PPECC was founded in response to a growing need for a forum in which engineers from all disciplines can meet with each other, and with parallel processing specialists, to seek guidance and impartial advice, compare notes, and benefit from each other's experiences.

A copy of the original announcement in ECN in May 1993 of the formation of PPECC may be found in Appendix 2a.

The aims of the Club at its foundation were:

- to bring together researchers seeking to exploit the potential of parallel processing in their own areas of research;
- to provide a forum for the exchange of practical experience about applications of parallel processing;
- to increase awareness of parallel processing and its potential through workshops, seminars, tutorials and courses;
- to identify requirements which can be met through the provisions of the EASE Programme;
- to encourage the emergence and use of relevant standards which will assist the development of software for parallel systems.

These aims are intentionally broad, to embrace both those who use parallel techniques for the most demanding applications, e.g. 'Grand Challenges', and those with more limited (but still substantial) demands, typical in embedded systems, in which once a basic solution is possible performance becomes a parameter of choice, or design, to be balanced against requirements, functionality, benefits and cost.

In practice, PPECC aims also to complement other initiatives in parallel computing, which mostly focus toward the higher end of the performance spectrum. The emphasis therefore of PPECC's activities has been toward small- and medium-scale 'embedded' systems, but with strong mutual interests with larger-scale high performance computing, e.g. in techniques for parallelisation and performance modelling.

At root, PPECC is about raising awareness and assisting people to exploit parallel processing in their own laboratories.

A general information sheet about PPECC may be found in Appendix 2b and further motivation in Appendix 2c.

3. MEMBERSHIP AND STEERING GROUP

3.1 Membership

Following the first registrations in June 1993, membership grew rapidly reaching 140 in September 1993 and 205 at the time of the formal Inaugural Meeting in June 1994. Steady growth since has taken the number of members to 271.

A questionnaire (see Appendix 3.1a) was sent to all members on enrolling. The responses provided much useful information in shaping the PPECC programme of events. (A full account of the questionnaire results was included in the Mailshot of August 1994 distributed to members.)

The most recent profile of members areas of interest has come from a validation exercise for ECN in Autumn 1994. The 158 PPECC subscribers to ECN who responded gave their areas of interest as shown in Table 1 (some had more than one).

Area	Number
Computer Science	54
Mechanical Engineering	30
Artificial Intelligence	28
Civil Engineering	25
Electronic Engineering	21
Electrical Engineering	20
Control Engineering	17
Process Engineering	16
Transport Engineering	14
Materials Engineering	8
Production Engineering	4

Table 1: Members Interests (Autumn 1994)

3.2 Steering Group

The activities of PPECC are co-ordinated by a Steering Group of representatives of the different engineering disciplines with an active interest in parallel processing. Its Terms of Reference are listed in Appendix 3.2a.

The initial Steering Group with 4 community members was recruited in March 1994, with Dr Brian Hoyle (University of Leeds) as Chairman. Two further members (one from industry) joined in September 1994. Membership of the Steering Group is completed by a cross-representative of the EPSRC CCP12 and HPCI initiatives, representative from EPSRC, and the RAL support staff. The full membership of the Steering Group is listed in Appendix 3.2b.

The Steering Group has met five times, in April, July and December 1994, May 1995, and February 1996. A brief meeting was also held following the PPECC Inaugural Meeting in June 1994.

4. ACTIVITIES SINCE MAY 1993

The main elements of the PPECC programme are

Events
- Seminars
- Workshops
- Courses

Case Studies

Assessment Reports

Parallel Evaluation Centre

Mailshot and Publicity

These were conceived at the outset and have come into activity progressively. Much of the effort available to date has gone into building up the events programme, particularly courses, during the period.

4.1 Seminars and Workshops

4.1.1 Inaugural Meeting

The Inaugural Meeting of the Parallel Processing in Engineering Community Club (PPECC) was held at the Rutherford Appleton Laboratory (RAL) on 1 June 1994.

The programme (see Appendix 4.1.1a) provided a mix of invited experts, presentations by PPECC support staff and finally an open discussion session.

The Meeting was chaired by the Steering Group Chairman, Dr Brian Hoyle., who drew attention in his opening remarks to the aims and focus of PPECC (see also Appendix 4.1.1b).

Three invited presentations were then given by Prof George Irwin, Dr Alastair Allen and Dr Dale King, each being active developers in engineering areas already exploiting parallel processing.

Prof George Irwin (Queens University Belfast) detailed his experiences with real-time control. Control mechanisms were increasingly more complex and now being located on each and every joint in a robotic arm. Higher level restraints such as "collision-free motion" were now being tackled using parallel techniques. The ease of expandability of parallel systems was shown to be highly relevant to the development of such systems.

Dr Alastair Allen (University of Aberdeen) showed that parallel processing had a natural match to the requirements for Image Processing. He indicated that researchers were increasingly turning to packages to assist in their developments and that these packages needed to start supporting and supplying parallel components.

Dr Dale King (British Aerospace) discussed how the drive for profitability demanded high performance computing requirements within the aeronautical industry. Currently most parallel computations were carried out on large scale systems and would in future move to the Massively Parallel Processing (MPP) systems.

Presentations were also given by RAL support staff on the structure, membership, future programmes and possible strategies for PPECC.

The meeting was closed with an extended open discussion of possible future activities and priorities. A lot of useful comments and suggestions were offered from the participants. Areas discussed included:

- *Focus*: What is the focus of PPECC? Should PPECC focus on Grand Challenge areas or the embedded field? Can PPECC cover such a large spectrum in an all encompassing fashion or seek to target specific areas in which to work? Where should PPECC seek to focus its efforts within this wide spectrum of parallel systems.

- *Liaison*: Establishment of links into other existing initiatives. Can PPECC bring together research and experts from current parallel initiatives to indicate future trends for parallelism?

- *Access*: on-line access route to and by members. Members requested on-line access routes to information on PPECC and related activities. Specific mention was made to the use of the email-list mechanism at mailbase. It was also pointed out that existing archives of parallel data/source/papers are available at University of Kent and wider dissemination of this would be useful.

- *Workshop Themes*: The discussion considered the case for a workshop on Embedded Systems, Distributed vs. Parallel, and Sequential vs. Parallelism. There was no overall consensus as to what theme should be selected.

55 members registered to attend, 7 of whom were 'no shows'. A list of those registered is in Appendix 4.1.1c.

A debriefing meeting was held of the Steering Group members present. This meeting concluded that the meeting had been a healthy start for the club and actioned several matters to be considered at the next Steering Group meeting.

4.1.2 Seminar on Embedded Parallel Processing

A seminar on *Embedded Parallel Processing* had been planned to be held on 23 February 1995 but failed to attract a sufficient number of registrations for a viable event.

The poor response was particularly disappointing. It was felt that a strong programme (see Appendix 4.1.2a) had been put together with an excellent booklet of some 120 pages of material to accompany the talks. The response was also surprising since members stated interests, and support expressed at the Inaugural Meeting, indicated that a seminar on this topic would be a popular one.

After canvassing about 20 members at random, it was decided to send a questionnaire (see Appendix 4.1.2b) to all members to seek to understand the reasons for the poor response. At the same time the opportunity was taken to enquire further about interests and preferences for seminars generally, including choice of venue and dates.

It was eventually decided not to reschedule the seminar for a new date but to make the booklet available to PPECC members. The booklet issued contains all the speakers' material except for one which was omitted for copyright reasons.

4.1.3 Seminar on Parallel Field Analysis in Engineering

The large majority of all supercomputer usage is on one form or another of field analysis, and this type of computation has become an important target for parallel machines.

A seminar on *Parallel Field Analysis in Engineering* was held at RAL on 11 July 1995 chaired by Dr Malcolm Sabin (Numerical Geometry Ltd and member of PPECC Steering Group). The seminar covered a wide range of applications (structural, crash-simulation, fluid dynamics, electromagnetics) and of solution techniques (finite elements, finite differences, boundary elements) including both explicit and implicit approaches and issues of mesh generation which can easily be the bottleneck for realistic problems. Both tightly coupled machines and the parallelism of multiple workstations were addressed. The final session included an overview of the Europort programme and an extended discussion session which further identified the significance of parallel processing for applications in this area.

The seminar was aimed to be of particular interest to engineers who are looking for ways of using parallel computing power to speed and extend their time-consuming analysis codes. The event attracted an audience of 29. Details of the programme may be found in Appendix 4.1.3a.

A booklet containing material provided by the speakers is available separately.

4.2 Workshop on Distributed vs Parallel

With the increasing use of both distributed computing environments and parallel processing environments by engineers, and the increasing commonality of interest between these, it was agreed that this would be a topical theme for a Workshop and the title *Distributed vs Parallel: convergence or divergence?* was chosen to provoke a lively debate. The event did not disappoint!

The Workshop was held on 14-15 March 1995 at the Cosener's House, Abingdon, chaired by Prof Peter Dew (University of Leeds). The event took the form of 4 invited presentations, 19 position papers (9 of which were selected for presentation), 3 parallel subgroups and a closing plenary session.

Copies of the Workshop Announcement and Call for Papers, Final Programme, and List of Attendees are attached as Appendices 4.2a, 4.2b, and 4.2c respectively.

A one-page report that appeared in the May 1995 issue of ECN is in Appendix 4.2d.

A full report of the Workshop is available separately.

4.3 Courses

Three two-day courses have been held, with descriptions and programme attached in the Appendices cited:

Parallel Fortran for Engineers	13-14 July 1994 & 14-15 June 1995	Appendix 4.3a
Parallel Processing Techniques	25-26 October 1994	Appendix 4.3b
Parallel C for Engineers	18-19 January 1995	Appendix 4.3c

The Fortran and C courses included hands-on elements which limited the number of places to 12. All 12 places will filled for the Fortran course. The C course had 9 attendees. The Techniques course had a nominal limit of 16 places but in the event was stretched to accommodate 19 attendees.

4.4 Technical Articles

Three technical articles have been written by RAL staff for ECN:

The New Kid in Parallel Processing, David Johnston, ECN 50 (May 94)

C for Parallelism, David Johnston, ECN 54 (Jan 95)

C++ *Parallel Systems*, David Johnston. ECN 55 (March 95)

Two articles written by members of the community have also been published in ECN:

An Overview of High Performance Fortran, Mike Delves (Liverpool), ECN 50 (May 94)

The Evolution of Parallel Operating Systems, Kevin Murray (City University), ECN 53 (Nov 94)

Copies of all these are available separately.

4.5 Parallel Evaluation Centre (PEC)

A Parallel Evaluation Centre (PEC) for use by the community was already in use at RAL when PPECC was announced in May 1993. The PEC is equipped with a range of small, low-cost systems for users to evaluate, which have been updated as significant new systems appear (and funding permits), much of these in the form of "add-ins" or "add-ons" to PCs or workstations. Typical costs are in the range £1K-£5K per node. Since 1994 the Centre has a number of i860-, C40- and transputer-based distributed memory systems, a Parsys Supernode, and a 4-processor, 486-based, shared memory multiprocessor, the latter running a multiprocessor version of Windows NT.

The PEC also provides access to information and impartial advice. This has been promoted regularly in ECN, with staff available at RAL to follow-up enquiries. Enquiries have ranged from simple e-mail enquiry and response, or gathering and disseminating information sought, to more extended discussion or a meeting with enquirers about requirements and techniques for their application, or "hands-on" assistance in using the kit in the PEC.

While there has been intermittent usage of the kit by members, insufficient networking capability has limited remote usage and generally meant that it has been necessary for clients to travel to the Centre to use the facilities effectively. This in turn has limited usage in practice.

Experience has shown that in the Community Club context it is the availability of skilled people to provide advice etc which has been of most value to clients of the Centre, particularly in getting started and in pointing to directions clients had not been aware of.

A copy of the PEC brochure is included in the publicity material in Appendix 4.6a.

4.6 Mailshot, Publicity and Liaison

Throughout the period the principal route for publicising PPECC activities has been the Engineering Computing Newsletter (ECN) in which PPECC has had a regular (2-monthly) column with additional items from time to time (e.g. Workshop report, and technical articles listed in Section 4.4). Announcements of PPECC events and booking forms have been provided routinely as inserts to ECN. Leaflet-style brochures for PPECC and PEC have been produced and widely distributed, see copies in Appendix 4.6a.

At the outset it was planned to distribute a (paper) Mailshot to members with lengthier and more detailed information and papers about twice a year. In the event one Mailshot was distributed in August 1994 but already by then the growth in electronic distribution, via email and especially the rapid growth in the Web, was making distribution by paper Mailshot twice a year out of date.

A PPECC Web page was established in 1994 and is accessible at

http://www.cis.rl.ac.uk/clubs/PPECC/index.html

This contains full information about PPECC and is updated regularly with notices and news of PPECC activities and of reports available (on line or separately).

An email reflector was also established in 1994 and enables direct email discussion with members registered with the reflector. Messages may be *sent* to those registered by sending an email to

ppecc@mailbase.ac.uk

To ***receive*** messages sent by others, it is necessary to register with mailbase first, by sending an email to

mailbase@mailbase.ac.uk

with content

`join ppecc <name> <surname>`

Liaison is maintained with closely related initiatives, notably the EPSRC High Performance Computing Initiative (HPCI) through representation on the Steering Group (Blake), the EPSRC Portable Software Tools for Parallel Architecture programme (PSTPA) through the Coordinator (first author - Wadsworth), and the BCS Parallel Processing Specialist Group of which the second author (Henderson) is Treasurer. PPECC support staff at RAL worked with the BCS group in putting together the event *Programming with Threads* held in London on 18 December 1995. Wadsworth has served on many Programme Committees/Advisory Boards during the period reported, currently for UKPAR'96 and EUROPAR'96 and for the journal Scientific Programming.

5. FUTURE PROGRAMME

During summer 1995, EPSRC carried out a review, based on a questionnaire to grantholders, of its EASE Community Clubs, including PPECC. As a result some continuing funding is being provided, on a reducing profile, with the expectation that each Community Club would evolve its own future beyond that.

The PPECC Steering Group discussed the future focus of PPECC at its meeting in February 1996. It felt that a widening in focus was both timely and appropriate. More especially, it felt that the concern now was less with the technology of parallel (and distributed) processing, more with techniques for solving computationally demanding problems (which because of their demands are likely to require parallel processing). A range of advanced techniques of topical interest was compiled, including:

Neural Computing
Genetic Programming and Genetic Algorithms
Evolutionary Computing
(Uses of) Fuzzy Logic
Advanced Simulation and Modelling
Embedded Systems Techniques
Real-Time Computing
Advanced Parallel/Distributed Computing

The Steering Group concluded that the evolution of focus was such that a change in the name of the Community Club was also appropriate and provisionally agreed a new title of

Advanced Computing Techniques Community Club (ACTCC)

It also concluded that the next event should be a "re-launch" event at which the views of the community would be sought in refining further the scope and future programme. This event is now being planned for the second half of July 1996.

6. FURTHER INFORMATION

Further information on any aspect of the PPECC may be obtained from the second author, Brian Henderson (PPECC Secretary and PEC Manager) by any of the following routes:

Post: Brian Henderson
Rutherford Appleton Laboratory
Chilton, Didcot
Oxon OX11 0QX

Tel: 01235 446151

Fax: 01235 445945

Email: ppecc@inf.rl.ac.uk (*preferred*)

Technical enquiries about parallel processing are also welcome and will be switched to the RAL support staff available as appropriate.

APPENDIX 1A. REPORTS AND ARTICLES

Workshop Report

1. *Distributed vs Parallel: convergence or divergence?*, Abingdon, 14-15 March 95

Seminar Booklets

2. *Inaugural Seminar*, RAL, 1 June 94
3. *Embedded Parallel Processing* (23 February 95)
4. *Parallel Field Analysis in Engineering*, RAL, 11 July 95

Course Notes

5. *Parallel Fortran for Engineers*, 13-14 July 94 & 14-15 June 95
6. *Parallel Processing Techniques*, 25-26 October 94
7. *Parallel C for Engineers*, 18-19 January 95

Mailshot

8. August 1994

ECN Articles

9. *The New Kid in Parallel Processing*, David Johnston, ECN 50 (May 94)
10. *C for Parallelism*, David Johnston, ECN 54 (Jan 95)
11. *C++ Parallel Systems*, David Johnston. ECN 55 (March 95)
12. *An Overview of High Performance Fortran*, Mike Delves (Liverpool), ECN 50 (May 94)
13. *The Evolution of Parallel Operating Systems*, Kevin Murray (City University), ECN 53 (Nov 94)

Copies of the above material, and of the regular PPECC columns in ECN, may be obtained from the PPECC support staff at RAL (see Section 6).

APPENDIX 2A. PPECC ANNOUNCEMENT

Following is a copy of the announcement of the formation of PPECC as it appeared on the front page of ECN in May 1993:

Engineering Computing Newsletter

SERC

The Newsletter of the Engineering Applications IT Support ProgrammE (EASE)

Rutherford Appleton Laboratory **Issue 44: May 1993**

Parallel Processing in Engineering Community Club being formed

Despite its relative lack of maturity, parallel processing is steadily gaining acceptance as a potentially cost effective solution to a range of computationally intensive engineering problems. Within the last year, a number of major established computer suppliers have announced new products incorporating parallel processing. Many of these are based on the new generation of powerful RISC processors linked together in a variety of ways. There are also increasing signs of convergence in the programming styles being supported.

An increasing number of engineering research grant-holders are proposing to use parallel processing techniques. With the rapid pace of development in parallel processing, and the wide and often confusing range of software techniques available, there is a growing need for a forum in which engineers from all disciplines can meet to seek guidance, compare notes and profit from each other's experiences.

To this end, a new Community Club on the topic of Parallel Processing in Engineering is being formed based on the successful model in other domains including Computational Fluid Dynamics and Visualization. The aims of this new Community Club will be:

- to bring together researchers seeking to exploit the potential of parallel processing in their own areas of research
- to provide a forum for the exchange of practical experience about applications of parallel processing
- to increase awareness of parallel processing and its potential through workshops, seminars, tutorials and courses
- to identify requirements which can be met through the provisions of the EASE Programme
- to encourage the emergence and use of relevant standards which will assist the development of software for parallel systems

The activities of the Community Club will be co-ordinated by a small Steering Group of representatives of the different engineering disciplines within the research community with an active interest in parallel processing.

The Parallel Processing Group at RAL will provide organisational and technical support for the activities of the Club. The Parallel Evaluation Centre established and operated by the Group will be available to members of the Club to try out a range of current affordable parallel hardware and software systems.

As a first step towards the formation of the Club, we are inviting engineering researchers with an interest in parallel processing to contact us, preferably by email, to register their interest. We will shortly be sending out a brief questionnaire to gather further information about current parallel processing activities within the engineering research community. If you would like to join the new Parallel Processing in Engineering Community Club please send a message including your address, phone and email details to ppecc@uk.ac.rl.inf (preferred) or contact me directly.

C P Wadsworth
Head, Parallel Processing Group
Informatics Department
RAL, Chilton, DIDCOT
Oxon, OX11 0QX
Tel: 0235 445101
Fax: 0235 445945

ALSO ...

Inserts:

Improving the Quality of Fortran Programs

Introduction to Human Factors Aspects of User Interface Design

If undelivered please return **directly** *to:*

Rachel Miles
RAL, Chilton
DIDCOT, OX11 0QX

APPENDIX 2B. PPECC INFORMATION SHEET

Benefits of Parallel Processing

Parallel processing is a means to an end. Engineers, like other users, are typically motivated by its potential benefits:

- to run existing applications *cheaper*
- to run existing applications *faster*
- to tackle *bigger problems*
- to add *more functionality* to existing applications
- to enable *new applications*

In short, better performance in one form or another.

Cost effective solutions

Parallel processing is gaining increasing acceptance as a cost-effective solution to a range of computationally intensive problems. More especially, systems built from many cheap microprocessors operating in parallel now offer an order of magnitude better *price/performance* than conventional uniprocessor systems. Within the last year, a number of major suppliers (IBM, Cray, Convex, Intel) have announced such systems. Lower down the scale, more modest-sized affordable parallel systems are also available commercially. There are also increasing signs of convergence in the programming styles being supported, with *de facto* standards emerging (e.g. HPF, PVM, MPI, VSM).

Engineering Applications

Within engineering, applications cover a wide spectrum of performance requirements, ranging from a few processors embedded in other equipment, e.g. in an on-line control system, to applications requiring the very highest performance attainable only with lots of processors, e.g. a large-scale simulation of a fluid flow problem. Embedded applications are particularly many and varied – in areas such as real-time control, signal processing, imaging, process control, telecommunications, consumer products – and well-matched to the low cost parallel hardware now available. Typical parallel designs might range from a few to a few dozen processors. The flexibility of parallel processing allows ready experimentation and optimisation in the tradeoffs between functionality, performance, and cost.

New Community Club

With the rapid pace of development, getting unbiased and up-to-date advice and assistance can be a problem for users more interested in their engineering problems than in the computing technology they need to use. To meet this need, a new *Community Club* on the topic of Parallel Processing in Engineering has been launched to bring together researchers seeking to exploit the

potential of parallel processing in their own areas of research.

The Club provides a forum for the exchange of practical experience and for the identification of requirements which can be met through the Club's programme. Seminars, Courses and other events are held regularly, either at RAL or at users' own sites if demand is sufficient. Club activities are co-ordinated by a Steering Group of representatives of the interested engineering disciplines within the research community.

Support for the Community Club is provided by the Parallel Processing Group in the Informatics Department and takes a number of forms:

- a *Parallel Evaluation Centre* has been established and is available to engineering researchers. The Centre is equipped with a range of affordable parallel hardware and software systems, much of this in the form of "add-ins" or "add-ons" to PCs or workstations. Currently the Centre has a number of i860-, C40- and transputer-based distributed memory systems, a Parsys Supernode, and a 4-processor, 486-based, shared memory multiprocessor.

- the staff of the Parallel Processing Group will assist users of the Centre and provide independent advice on parallel processing techniques and choice of hardware and software.

- Assessment Reports on significant new developments of interest to the community are produced from time to time.

- a series of Case Studies is being started on the application of parallel processing to engineering research problems. These will be developed in conjunction with users, and focus on the contribution of parallel processing in solving the engineering problem and on the methods followed in practice.

Further Information

If you would like to join the Community Club, or receive information about the Centre facilities and other activities, please send an email message (strongly preferred) including your name, address, phone, fax, and email details to *ppecc@inf.rl.ac.uk* or contact either of us directly.

Dr C P Wadsworth, Group Leader — Tel: 01235 44 5101
Mr B W Henderson, PPECC Secretary — Tel: 01235 44 6151

Parallel Processing Group
Informatics Department
Rutherford Appleton Laboratory
Chilton, Didcot
Oxon OX11 0QX

Fax: 01235 44 5945
Email: ppecc@inf.rl.ac.uk

APPENDIX 2C. PPECC BACKGROUND AND PROGRAMME ELEMENTS

Introduction

Within engineering, applications cover a wide spectrum of performance requirements, ranging from a few processors embedded in other equipment, e.g. in an on-line control system, to applications requiring the very highest performance attainable only with lots of processors, e.g. a large-scale simulation of a fluid flow problem. Embedded applications are particularly many and varied – in areas such as real-time control, signal processing, imaging, process control, telecommunications, consumer products – and well-matched to the low cost parallel hardware now available.

Support for Parallel Processing under the EASE Programme (EASE PP) addresses the need for local, affordable parallel computing, e.g. for an embedded or special-purpose application, to integrate with other local facilities, or to provide a dedicated local system when this is the most cost-effective solution.

Performance remains a dominant consideration, but often in a markedly different sense: typically, once a performance constraint (e.g. a real-time response in a process control application) is met, there is little advantage in further speed-up. Advantage is gained, however, by placing processing where it is needed (and up to the amount that is needed) and then optimising. Typical parallel designs might range from a few to a few dozen processors. The flexibility of parallel processing allows ready experimentation and optimisation in the tradeoffs between functionality, performance, and cost. In some cases there may be additional constraints, e.g. low power consumption. Ultimately for a production system the engineer seeks maximum functionality meeting required performance constraints for minimum cost.

Focus of Programme

The EASE PP programme focuses on assisting engineering researchers and users to exploit parallel processing in their own laboratories, with emphasis on choice and use of suitable hardware and software and on increasing the community's awareness of relevant parallel processing techniques including the issues of portability and scalability.

The emphasis is toward affordable, modest-sized parallel systems which may be installed cost-effectively as an "add-in" or "add-on" to existing systems (typically PCs or SUN workstations) or for integration in custom or embedded designs. Assistance is also provided with getting started, with advice on choosing suitable configurations, and with advice on approaches that minimise dependence on current choices in an area in which the technology is changing rapidly.

Community Club (PPECC)

The Parallel Processing in Engineering Community Club (PPECC) has been established to guide the EASE PP programme and provide a channel for increased feedback from and to the community. A Steering Group drawn from interested engineering disciplines has been formed following the successful models of the CFD and Visualisation Community Clubs.

Membership now[1] stands at 205 members. On registration members have been sent a

1. June 1994

questionnaire about their interests in PP and preferences for events that PPECC might run. (An analysis of the responses is being presented separately at the Inaugural Meeting.) PPECC events are routinely advertised in the Engineering Computing Newsletter (ECN). A PPECC Mailshot is also planned to disseminate more particular information.

Parallel Evaluation Centre (PEC)

A Parallel Evaluation Centre (PEC) for use by the community was set up at RAL in 92/3 and is now equipped with a range of transputer, i860 and C40 distributed memory systems, a 486-based shared memory system, and appropriate up-to-date software (including, e.g., multiprocessor Windows NT on the 486 system). This provides a range of small, low-cost systems for users to evaluate, which are updated as significant new systems appear. Typical costs are in the range £1K-£5K per node.

The PEC also provides access to information and impartial advice. It is promoted regularly in ECN, with staff available at RAL to follow-up enquiries. This may range from a simple e-mail enquiry and response, or gathering and disseminating information sought, to more extended discussion or a meeting with enquirers about requirements and techniques for their application, or "hands-on" assistance in using the kit in the PEC.

Experience has shown that the availability of skilled people to provide advice etc is at least as valuable to clients of the Centre as the availability of kit for evaluation, often pointing clients in directions they had not been aware of.

Technical Meetings

Three kinds of technical meetings may be distinguished in the PPECC Programme:

Seminar: a programme of talks on a chosen topic, generally with a mix of speakers (usually 1 day)

Course: more specific training on a technical topic, possibly with "hands on" (1-5 days)

Workshop: a mix of talks and discussion sessions on a chosen theme, generally with a purpose of drawing conclusions and recommendations (1 or 2 days)

Seminars and Workshops are generally designed for audiences of 30 or more (but not too much more for Workshops), whereas Courses may be more limited in number of participants particularly if "hands on" practicals are included (max 12 people currently using the PEC facilities). Courses are designed to be repeatable, with new training material developed as required to complement existing documentation or papers. Recent courses have been consistently oversubscribed, ensuring an immediate demand for the next run. Workshops have been held about once a year on a currently topical theme (most recently, on "Developing Parallel Engineering Applications" held in February 1993). Seminars concerned with PP have to date been held under the more general remit of the EASE Education and Awareness Programme.

Topics for future events will be defined by the PPECC Steering Group taking account of the views of the community. The questionnaire responses already provide useful guidance. Two high-points are noticeable: first, a strong demand for "how to" events on exploiting the technology (Parallel Programming Techniques, Parallel Program Development, Developing for Performance) and, second, a demand for update seminars on PP technology, particularly software. There is also a high aggregated demand for seminars on experience in specific

application areas, though further analysis is needed to identify those areas for which the demand is greatest. Some events may be more appropriately planned as Workshops where future directions need to be established. Close liaison with the needs of interested engineering programmes is maintained through the Steering Group members.

The current level of demand indicates that Seminars should be held about once a quarter, Courses repeating three times a year, and Workshops at least once a year. It is doubtful whether this number of events could be sustained along with the other activities within the current effort allocation. The Steering Group will need to assess the relative priorities.

Case Studies

A growing body of case studies on the application of parallel processing systems to engineering research problems will be developed in conjunction with users. The studies will focus on the contribution of parallel processing in solving the engineering problem (rather than the engineering problem per se) and on the methods followed in using parallel processing in practice, in particular its role in design decisions and tradeoffs, and experience with the hardware and software products used. Choices which were considered but rejected will be reported as well as those which were eventually taken. The engineering benefits and the development experience will also be stressed.

Such material is still largely lacking, particularly for engineering-oriented problems. However existing users have gained much practical experience which will be of benefit to others. The results will be disseminated as exemplars of best practice - how to do it and, indeed, some lessons on how not to do it.

Assessment Reports

Assessment reports of significant new developments of interest to the community are produced from time to time. Two are already well advanced: a report on the use of i860s in parallel systems for engineering applications, and a report on message passing software (PVM) to support the use of coupled workstations as a parallel computing resource. Occasionally reports addressing more strategic issues are produced, e.g. a report in preparation on the emerging standards and trends in parallel processing with suggestions on a viable "intercept" strategy for a 1-2 year timeframe and beyond. Reports on multiprocessor operating systems and on "Getting Started with PP" are also being considered.

APPENDIX 3.1A. QUESTIONNAIRE ON ENROLLING

Questionnaire - Parallel Processing in Engineering Research

A Community Club on Parallel Processing in Engineering has recently been launched, co-ordinated by the Parallel Processing Group at RAL. Its brief is to bring together and assist researchers seeking to exploit the potential of Parallel Processing (PP) in their own areas of research. A fuller description of its aims may be found in the latest issue (May 1993) of the SERC Engineering Computing Newsletter.

This questionnaire is designed to find out more about current (or prospective) PP activities within the engineering research community and about your preferences for events that the Community Club may run. *Please complete and return this form if you are interested in PP and/or wish to become a member of the Community Club. Please expand or give any other views on priorities for the Community Club on a separate sheet if you need more space.*

Name (incl Title): _____

Department/Area of Work: _____

HEI/Company: _____

Address: _____

_____

_____

Post Code: _____

Telephone: _____ Fax: _____

Email: _____

SERC Grant Number(s): _____

SERC Committee awarding grant: _____

I. About you

With regard to PP, would you describe yourself primarily as ...

O User O Developer O Interested in finding out more

What engineering applications do you (would you) use PP for? _____

_____

Which of the following areas do you use PP for (1 or more)?

O Image Processing
O Signal Processing
O Simulation
O Modelling
O Real-time
O Device control
O Process control
O Embedded systems

O other (*please specify*) _____

Which of the following best describe your motivation for using/interest in PP?

- O to run existing applications *cheaper*
- O to run existing applications *faster*
- O to tackle *bigger problems*
- O to add *more functionality* to existing applications
- O to develop *new applications*
- O other (*please specify*) _____

Please summarise the particular PP techniques that you are using (expect to use) and whether, in your experience, these favour choice of particular parallel architectures/machines.

_____

_____

_____

If already using PP, what hardware and software do you use? _____

_____

_____

_____

II. Events

The Community Club expects to run a mix of Seminars, Courses, and Workshops, disambiguated as follows:

Seminar:	a programme of talks on a chosen topic, generally mix of speakers (usually 1 day)
Course:	more specific training on a technical topic, possibly with "hands-on" (1-5 days)
Workshop:	a mix of talks and discussion sessions on a chosen theme, generally with a purpose of drawing conclusions and recommendations on priorities (1 or 2 days)

There is a possibility of holding Courses, and possibly Seminars, at your own site if there is a sufficient quorum (say 10 for Courses, 20 for Seminars). *For the questions in this part please show your preference/interest on a scale from 1 (low) to 5 (high).*

Please grade your interest in the 3 types of events:

Seminars	1	2	3	4	5
Courses	1	2	3	4	5
Workshops	1	2	3	4	5

Please grade your interest in possible **Seminar** topics:

PP Awareness	1	2	3	4	5
PP Technology Update - Hardware	1	2	3	4	5
PP Technology Update - Software	1	2	3	4	5
Choosing a Parallel System	1	2	3	4	5
Parallel Programming Techniques	1	2	3	4	5
Parallel Program Development	1	2	3	4	5
Developing for Performance	1	2	3	4	5
Experience with Applications - general	1	2	3	4	5
Experience with Applications - specific area	1	2	3	4	5

state area: _____

other (*specify*) _____

Please grade your interest in possible Course topics, possibly with "hands-on":

Parallel Fortran	1	2	3	4	5	hands-on?
Parallel C	1	2	3	4	5	hands-on?
Occam	1	2	3	4	5	hands-on?
Transputers	1	2	3	4	5	hands-on?
Techniques for Exploiting PP	1	2	3	4	5	hands-on?
Applications of PP	1	2	3	4	5	hands-on?
other (*specify*) _____						hands-on?

What would be you preferred length of courses?

With "hands-on"	1	2	3	4	5	(days)
Without "hands-on"	1	2	3	4	5	(days)

Please suggest themes for Workshops that would be of interest to you _____

_____

_____

How important do you regard the following in the context of PP:

Performance	1	2	3	4	5
Efficiency	1	2	3	4	5
Portability	1	2	3	4	5
Ease of use	1	2	3	4	5
Ease of development	1	2	3	4	5
Transparency (hiding parallelism)	1	2	3	4	5
Unified programming basis	1	2	3	4	5
Performance modelling	1	2	3	4	5
Performance prediction	1	2	3	4	5

III. Community Club

Do you want to join the PP in Engineering Community Club? yes / no

I understand that the information given above will be stored in a computer file.

Signed: _____ Date: _____

APPENDIX 3.2A. TERMS OF REFERENCE OF PPECC STEERING GROUP

(revised July 1994)

1. To advise the Rutherford Appleton Laboratory on running an EASE Community Club in Parallel Processing in Engineering (PPE).

2. To make recommendations on a programme of activities to benefit the PPE research community.

3. To maintain knowledge of methods and techniques in parallel processing with particular relevance to engineering applications.

4. To monitor the provision and use of parallel computing facilities by engineering researchers.

5. To encourage interchange of ideas and knowledge between engineers and parallel processing providers.

6. To liaise with other parallel processing initiatives in the UK as appropriate.

7. To establish links with industry to ensure that industry and academia are each conversant with the requirements and activities of the other.

8. To report to the Community Club in PPE at least annually.

9. To report through relevant Programme Managers to the Head of the Core Engineering Programmes on the activities of the Community Club and on the provision and use of facilities for PPE at least annually.

APPENDIX 3.2B. MEMBERSHIP OF PPECC STEERING GROUP (1 April 1995)

Dr J D (Puff) Addison
Centre for Transport Studies
Dept of Civil & Environmental Engineering
University College London
Gower Street
London WC1E 6BT
Tel: 0171 387 7050, x2087
Fax: 0171 383 5580
Email: puff@transport.ucl.ac.uk

Prof K N C (Ken) Bray
Dept of Engineering
University of Cambridge
Trumpington Street
Cambridge CB2 1TZ
Tel: 01223 332744
Fax: 01223 332662
Email: janis@eng.cam.ac.uk

Dr G S (Grahame) Cooper
IT Institute
University of Salford
The Crescent
Salford M5 4WT
Tel: 0161 745 5759
Fax: 0161 745 8169
Email: G.S.Cooper@iti.salford.ac.uk

Dr B S (Brian) Hoyle
Dept of Electronic & Electrical Engineering
University of Leeds
Leeds LS2 9JT
Tel: 0113 233 2056
Fax: 0113 233 2032
Email: B.S.Hoyle@leeds.ac.uk

Dr B A (Brian) Murray
MTD Ltd
Innovation Centre
Exploration Drive
Offshore Technology Park
Bridge of Don
Aberdeen AB23 8GX
Tel: 01224 827005
Fax: 01224 827017
Email: B.A.Murray@aberdeen.ac.uk

Dr M (Malcolm) Sabin
26 Abbey Lane
Lode
Cambridge CB5 9EP
Tel: 01223 812721
Fax: 01223 812721
Email: malcolm@geometry.demon.co.uk

Dr R J (Richard) Blake
Daresbury Laboratory
Warrington WA4 4AD
Tel: 01925 603372
Fax: 01925 603634
Email: R.J.Blake@daresbury.ac.uk

Miss R M (Ros) Eden
EPSRC
Polaris House
North Star Avenue
Swindon SN2 1ET
Tel: 01793 411829
Fax:
Email: R.M.Eden@epsrc.ac.uk

Dr C P (Chris) Wadsworth
RAL
Chilton, Didcot
Oxon OX11 0QX
Tel: 01235 445101
Fax: 01235 445945
Email: cpw@inf.rl.ac.uk

Mr B W (Brian) Henderson
RAL
Chilton, Didcot
Oxon OX11 0QX
Tel: 01235 446151
Fax: 01235 445945
Email: bwh@inf.rl.ac.uk

APPENDIX 4.1.1A. INAUGURAL MEETING PROGRAMME

Parallel Processing in Engineering Community Club

Inaugural Meeting

Chairman: Dr Brian S Hoyle, University of Leeds

R22 Lecture Theatre, Rutherford Appleton Laboratory
Wednesday 1 June 1994

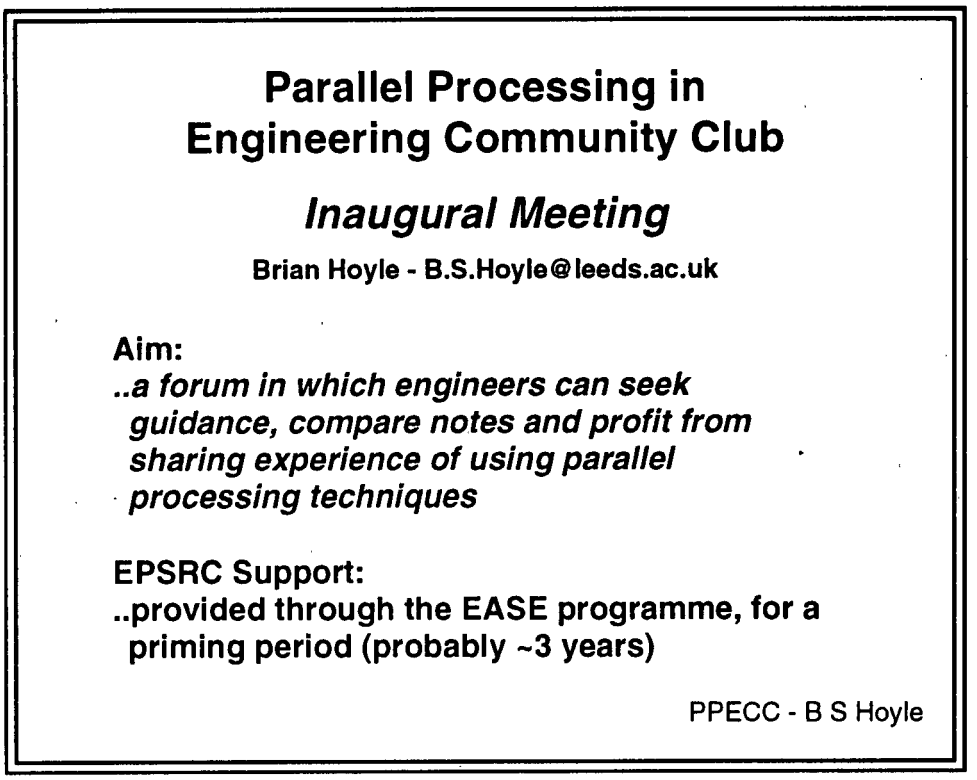
The Parallel Processing in Engineering Community Club (PPECC) has been formed to meet a growing need for a forum in which engineers from all disciplines can meet to seek guidance, compare notes and profit from each other's experiences of using parallel processing techniques.

The programme for this Inaugural Meeting includes items on the background and future activities of the Community Club, three presentations on experiences of using parallel processing, and a strategic overview of recent developments in parallel computing technology particularly software. The results of a questionnaire to members will also be presented, and there will be opportunities for discussion including a closing session on how the Club can best meet the community's needs.

The meeting will be of interest to all engineers who are using, or considering using, parallel processing in their research.

1000	Registration and Coffee
1030	**Welcome and Introduction** *Dr Brian Hoyle, University of Leeds*
1045	**PPECC Background and Purpose** *Dr Chris Wadsworth, RAL*
1110	**Results of Members' Responses to Questionnaire** *Mr Brian Henderson, RAL*
1130	**Experiences in Real-Time Control** *Prof George Irwin, Queen's University Belfast*
1200	Discussion
1205	**Parallel Signal and Image Processing** *Dr Alastair Allen, University of Aberdeen*
1235	Discussion
1240	Lunch
1345	**An Industrial Perspective** *Dr Dale King, British Aerospace*
1415	Discussion
1420	**Parallel Computing Strategy and Software Standards** *Mr David Johnston, RAL*
1450	Discussion
1455	Tea
1515	**PPECC Programme 1994/95** *Dr Chris Wadsworth, RAL*
1530	**Open Discussion on PPECC Programme**
1615	Close

APPENDIX 4.1.1B. CHAIRMAN'S REMARKS



The aim of the Community Club is wide ranging and seeks to address the interests of the engineering community at large with general interests in parallel processing techniques. The aim is intentionally broad to include those who use parallel techniques to solve relatively large problems on parallel computers, for example in modelling and simulation, to those whose target products and systems include substantial parallel processing. Where interests lie in modelling and simulation applications the Club is likely to offer a forum for the exchange of techniques for parallelisation and performance comparison. Hence there will be strong mutual interests with others working on embedded systems and vice versa.

Support for the Community Club is currently provided by the EASE/IT Awareness programme, whose brief is to enhance the awareness and high qulaity application of IT in engineering research programmes. The programme is currently managed in EPSRC by a Programme Manager who is advised by a small Steering Panel. The programme is intended to support the wider community rather than individuals and does not have a responsive grant programme. Recent indications are that Community Clubs will be funded as 'pump priming' activities to establish links between researchers and industry and promote the exchange of information. In the first instance this period is likely to be 3 years.

Background and Expectations

- **UK has pioneering background: Manchester, Inmos** (e.g. *Parallel Computers 2*, Hockney & Jesshope)
- **Previous SERC/DTI programmes: Transputer Initiative** (e.g. *Transputer Applications - progress and prospects*, Jane, Fawcett and Mawby; *Transputers in Real-time Control*, Irwin & Fleming)
- **Experience from other CCs: CFDCC, Visualisation CC**
- **Parallel processing in engineering: real-time control, signal and image processing, industrial perspectives, software tools....**
- **What next...?**

The UK has an enviable history in the development and novel application of computer systems, although, in common with many innovations has failed in many cases to capitalise at an early stage in their exploitation. Community Clubs offer a direct communication link between researchers and industry. They can help industrialists to learn of developments and help researchers to hear of industrial interests and requirements.

The recent Transputer Initiative was held by many researchers and industrialists to be a successful example of such a community programme, although of course this was specific to a single technology.

Other community clubs, in Computational Fluid Dynamics and in Visualisation have been successful in building strong and valuable links and provide a sound foundation of experience for the PPECC.

The Inaugural Meeting provides an initial opportunity to present some ideas on parallel processing; within the short time availabale a wide sample of work will be introduced: in real-time control, in signal and image processing and in aerospace modelling and simulation.

An initial programme has been prepared by the team, input from Club members is vital to ensure that planned activities are relevant. We also need to encourage all those with an interest to join, in particular colleagues in industry who are applying parallel techniques.

APPENDIX 4.1.1C. ATTENDEES AT INAUGURAL MEETING

Dr J D Addison	Centre for Transport Studies	University College London
Dr R K Aggarwal	School of Electrical Engineering	University of Bath
Dr A R Allen	Dept of Engineering	University of Aberdeen
Mr R Allison		Silicon Graphics
Mr P Anderton	Product Marketing manager	Silicon Graphics
Dr M T Arthur	Dept of Aerodynamics	Defence Research Agency
Dr A Bargiela	Dept of Computer Science	Nottingham Trent University
Mr M I Barlow	Engineering Design Centre	University of Newcastle
Ms C Barnes		EPSRC
Mr D Beckett	Computing Laboratory	University of Kent
Dr Janusz Bialek	School of Eng and Computer Studies	University of Durham
Dr D R S Boyd	Informatics	DRAL
Dr N Bridgett	Dept of Aeronautics and Astronautics	University of Southampton
Dr A F Clark	Electronic Systems Engineering	University of Essex
Dr D Crosta	Dept of Civil & Environmental Eng	University College London
Dr S Dobson	Informatics	DRAL
Dr R W Dunn	School of Electrical Engineering	University of Bath
Miss R M Eden		EPSRC
Dr H Ekerol	School of Manufacturing and Mech Eng	University of Birmingham
Mrs Susan Field		AEA Technology
Mr H Glaser	Electronics and Computer Science	University of Southampton
Dr P W Grant	Dept of Maths and Computer Science	University College Swansea
Dr M Greaves	School of ChemicalEngineering	University of Bath
Mr D Grey	School of Eng and Computer Studies	University of Durham
Mr B W Henderson	Informatics	DRAL
Dr D C Hodgson	Dept of Mechanical Engineering	University of Birmingham
Dr B S Hoyle	Dept of Elec & Elec Engineering	University of Leeds
Prof G W Irwin		Queen's University Belfast
Mr D J Johnston	Informatics	DRAL
Dr D I Jones	School of Electronic Eng Science	University College Bangor
Dr Dale King	Research Department	British Aerospace CAD
Dr G Makinson		University of Kent
Mr I Masters	Dept of Civil Engineering	University College Swansea
Mr R L Mattheys		British Gas plc
Mr J R Meneghini	Dept of Aeronautics	Imperial College
Mr J V Miro	Faculty of Technology	Middlesex University
Dr B A Murray	Innovation Centre	Marine Technology Dir Ltd
Dr C Pain	Dept of Mechanical Engineering	Imperial College
Mr B Parkinson	Maufacturing Eng Division	University of Hertfordshire
Dr J Piggott	Applied Computing Technology Group	British Gas
Mr K Pollmeier	Dept of Mechanical Engineering	University of Bath
Dr M Punjani	Dept of Engineering Computing	University of London
Dr J A Sharp	Dept of Computer Science	University College Swansea
Mr R A Shaw	Dept of Electrical & Electronic Eng	Nottingham Trent University
Mr T Short	Civil Eng Dept	City University
Mr A Taholakian	School of Engineering	Sheffield Hallam University
Dr H R Thomas	School of Engineering	University College Cardiff
Dr H A Thompson	Dept of Automatic Control and Sys Eng	University of Sheffield
Mr H T Tillotson	School of Civil Engineering	University of Birmingham
Mr V Trenkic	Dept of Electrical Engineering	University of Nottingham
Dr D Tsaptsinos	SEL-HPC Centre	QMW College London
Dr C P Wadsworth	Informatics	DRAL
Mr P A Wilson	Dept of Ship Science	University of Southampton
Dr X Zhang	Dept of Computer Science	University of Swansea

APPENDIX 4.1.2A. PROGRAMME FOR EPP SEMINAR

Following is a copy of the programme for the seminar on *Embedded Parallel Processing* that had been planned for 23 February 1995:

Parallel Processing in Engineering Community Club

One-day Seminar on Embedded Parallel Processing

Rutherford Appleton Laboratory
23 February 1995
Programme

As embedded systems become more and more advanced, so do their processing demands, often against real-time or other constraints (e.g. cost, size, power consumption). Parallel processing is opening new opportunities, both in enhancing the capability of existing systems (e.g. functionally or performance), and in developing new applications not otherwise feasible at acceptable cost.

The seminar reports on some of the latest work at the forefront of the exploitation of parallel processing in embedded systems research. The programme includes talks covering three prominent areas - control, signal processing and image processing- and a talk on the issues in porting real applications to embedded systems. There will be opportunities for discussion following each talk and an extended discussion session at the end. The seminar will be of particular interest to all engineers who are using, or considering using, parallel processing in their embedded system research.

9:45 - 10:15	*Coffee and Registration*
10:15 - 10:20	Welcome and Introduction Prof. George Irwin, Queen's University, Belfast.
10:20 - 11:05	"Application of parallel processing in real-time control" Dr. Haydn Thompson, University of Sheffield.
11:05 - 11:50	"Real-time optimal control on parallel transputer hardware" Dr. Dietmar Neumerkel, Daimler-Benz AG.
11:50 - 12:35	"An embedded transputer architecture for the control and guidance of high speed autonomous vehicles" Dr. Hugh Durrant-Whyte, University of Oxford.
12:35 - 12:40	Discussion - morning talks
12:40 - 13:30	*Lunch*
13:30 - 14:15	"Porting real application codes: from conception to embedded system" Mr. Hugh Webber, DRA Malvern.
14:15 - 15:00	"Structured parallelisation of embedded vision algorithms " Dr. Andy Downton, University of Essex.
15:00 - 15:20	*Tea*
15:20 - 16:05	"Parallel implementation of real-time process tomography" Dr. Bryan Hoyle, University of Leeds.
16:05 - 16:30	Open discussion
16:30	*Departure*

Engineering and Physical Sciences Research Council

Engineering Applications IT Support ProgrammE (EASE)

APPENDIX 4.1.2B. QUESTIONNAIRE ON PPECC SEMINARS

PART A. SEMINAR ON "EMBEDDED PARALLEL PROCESSING"

A1. *Were you aware of the planned Seminar?*
(copy of announcement attached)

- o YES, aware
- o NO, not aware

If NO, go to A5.

A2. *By which routes did you hear of the Seminar?*
(tick all that apply)

- o insert in ECN
- o PPECC Mailshot
- o ppecc@mailbase.ac.uk
- o direct email
- o word of mouth
- o other (*please specify*) _____

A3. *Were you registered (speaker or registrant) to attend?*

- o YES, registered
- o NO, not registered

If YES, go to A5.

A4. *For which reasons were you not registered?*
(tick all that apply, **and** circle most significant)

- o topic not of interest
- o programme not of sufficient specific interest (*)
- o registration fee
- o travel costs
- o date infeasible
- o venue infeasible
- o winter travel risks
- o university term time
- o school half term week
- o other (*please specify*) _____

(*) *If you ticked this box, please suggest other talks/speakers within the overall theme of Embedded Parallel Processing:* _____

_____

_____

_____

A5. *If the seminar were to be rescheduled, how likely would you be to attend (assuming date/venue are suitable)?*

- o very likely
- o possibly
- o not interested

A6. *If 'very likely' or 'possibly' ticked in A5, which of the following venues would be suitable for you?*
(tick those that are possible, **and** circle preferred)

- o RAL
- o London
- o North (Manchester/Leeds)
- o Central Scotland

PART B. FURTHER SEMINARS

B1. TOPICS: *Which of the following suggested seminar topics would be of interest to you?* Please tick to indicate some interest, **and** circle to emphasise high interest:

- o embedded parallel processing
- o parallel field analysis in eng.
- o technology update (including s/w availability)
- o migrating between systems
- o SQL awareness and use
- o impact of parallel and distributed operating systems/environments (user focus)
- o other (*please suggest*)

_____

_____

_____

B2. JOINT EVENTS: *Do you have contacts with other organisations that may be of interest for running a joint event?* Please give brief details of organisation and possible topics that could be followed up through yourself initially: _____

_____

_____

_____

B3. VENUES: *Please tick those which are possible for you, **and** circle the one that is most convenient.*

- o Central Scotland
- o North East
- o Central Northern England
- o Midlands
- o London
- o RAL

B4. DATES: The Community Clubs normally aim to schedule events outside university term time and avoiding school holidays and half-term breaks, but this is not always possible (it leaves very few days!) Fridays are also usually avoided.
*Please **mark 'X'** against any of the following descriptions that are regularly **impossible or difficult** for you.*

- _ University terms
- _ School holidays
- _ School half-terms
- _ Winter (Jan-March)
- _ Spring (April-May)
- _ Early Summer (June-midJuly)
- _ Late Summer (lateJuly-Aug)
- _ Autumn (Sept-Nov)
- _ pre-Christmas (December)
- _ other (*please specify*)

_____

PART C. PUBLICITY CHANNELS

PPECC events are routinely publicised in ECN, in the PPECC Mailshot, and via mailbase[1], with further event-specific promotion as appropriate.

C1. *Please list any other routes that would be useful for promoting PPECC events, either in general or for specific topics:* _____

_____

_____

_____

C2. *Were you aware of the email reflector 'ppecc@mailbase.ac.uk' ?*
- o YES, aware
- o NO, not aware

C3. *Are you registered to receive from the reflector?*
- o YES, registered
- o NO, not registered

C4. *If NO, why not?*
- o don't use email
- o would prefer a newsgroup (rather than a reflector)
- o other (*please specify*) _____

PART D. YOU (*OPTIONAL*)

Your name: _____

Organisation: _____

Tel: _____

Email: _____

PART E. REPLY TO

If you have any queries please contact Brian Henderson (Tel: 01235-446151, Email: ppecc@inf.rl.ac.uk) to whom completed questionnaires should be returned at

Brian Henderson
Rutherford Appleton Laboratory
Chilton, Didcot,
Oxon OX11 0QX

For maximum value please send responses ***by Friday 28 April 1995.***

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1. The email reflector *ppecc@mailbase.ac.uk* was established following requests at the Inaugural Meeting and is the quickest route for us - and members! - to communicate with each other, but its effectiveness to date has been limited by the numbers registered (about a quarter of members). To register, send a two-line message to *mailbase@mailbase.ac.uk* with the following body (note - both lines needed):

```
join ppecc <your first name> <your second name>
stop
```

APPENDIX 4.1.3A. PARALLEL FIELD ANALYSIS SEMINAR

Programme (Tuesday 11 July 1995)

0945	Registration and Coffee
1015	**Welcome and Introduction** *Dr Malcolm Sabin,* Numerical Geometry Ltd
1020	**Domain Decomposition and Parallel Non-Linear Finite Element Analysis** *Prof Barry Topping,* Heriot Watt University
1105	**Issues in Parallelising an Explicit Finite Element Code with contact-impact** *Dr Guy Lonsdale,* ESI GmbH
1150	**The HPCN gap: Is analysis the bottleneck?** *Dr P Harriss,* FEGS Ltd
1235	Discussion - morning talks
1240	Lunch
1330	**Tools for Parallelising Field Analysis Codes** *Prof Mark Cross,* University of Greenwich
1415	**Parallelising the Boundary Element Solution** *Dr R Adey,* Computational Mechanics Ltd
1500	Tea
1520	**Europort 1** *Dr Owen Thomas,* GMD
1605	**Open Discussion**
1630	Close

APPENDIX 4.2A. WORKSHOP ANNOUNCEMENT

Following is the announcement and call for position papers for the Workshop held in March 1995:

Parallel Processing in Engineering Community Club (PPECC)

WORKSHOP: "Distributed vs Parallel: convergence or divergence?: Call for Papers"

The Parallel Processing in Engineering Community Club (PPECC) is organising a Workshop on "Distributed vs Parallel: convergence or divergence?" to be held at The Cosener's House, Abingdon, on Abingdon, 14-15 March 1995. The Workshop will be chaired by Professor Peter Dew (University of Leeds).

Scope

There is a widespread acceptance that high performance computing environments are needed to solve a wide range of problems arising in science and engineering. Typical applications can be classified as:

* Computationally intensive
  (e.g. complex simulations)
* Data intensive
  (e.g. patterns in large databases)
* Real-time/response intensive
  (e.g. embedded systems, interactive visualisation, virtual reality)

In recent years there have been significant advances in the technology to handle these applications. Parallel computers are now much more widely available and with the emergence of high speed networks (e.g. FDDI and ATM) these computers can be connected into high performance distributed computing environments. This brings about a convergence of the issues being addressed by the Distributed and Parallel Computing communities. The widespread use of message passing (e.g. PVM and MPI) provides a common software platform where applications can be developed on a network of workstations and PCs (clusters) and ported to massively parallel processors (MPP) for production runs. The prospect of a "seamless" integration offering transparent and scalable migration of applications from clusters through to MPPs is becoming very attractive to users.

Differences do remain, however, at least in use. Distributed computing has traditionally focused on distributed *access*, local or geographically remote, typically with a single locus of control at any one time (e.g. remote procedure call) rather than concurrent activity on multiple nodes. Fault tolerance and the management of systems with multiple administrative domains have been a particular concern of distributed systems. Parallel computing has focused on *concurrent processing* and emphasised the goal of scalability to high levels of performance.

Perceived difficulties in developing applications, and in the limited range and level of available software tools, have also limited exploitation of these technologies to date.

How does the user respond to the changes in parallel and distributed computing? How much does the application programmer need to be aware of the differences? What differences remain? Which will persist? Are they differences of kind? Or of degree? Or of concern? What software tools would further assist the exploitation of either/both?

The objectives of the Workshop are:

* to pool experience from development and use of distributed systems and of parallel systems; and identify the state of the art.
* to identify future directions, needs and priorities for use in engineering applications
* to predict and potentially influence future trends
* to provide a forum for exchange of views between users, application developers, and technology specialists.
* to identify the educational and training needs of the community.

Topics of interest include (but are not limited to):

* Practical experiences of developing applications for distributed and/or parallel systems (with particular interest in experiences of using both)
* User views on the requirements and priorities for developing applications and supporting smooth migration between systems
* Software tools for distributed and/or parallel applications
* Portability and scalability across distributed and parallel computers
* Standards for heterogenous parallel systems
* Management of distributed and parallel systems
* Priorities for all types of applications, e.g. scientific, engineering, commercial, industrial

Workshop Format

The programme will consist of selected presentations from position papers, a small number of invited presentations from keynote speakers, discussion sessions in subgroups, and a closing plenary session. The number of places is limited (about 45) to foster active participation by all. A booklet of position papers will be distributed three weeks before the Workshop. A report will be produced containing the conclusions of the discussion sessions.

The Workshop will start mid-morning on 14 March and end mid-afternoon on 15 March. The fee for attending the Workshop will be £95 including accommodation at Cosener's House for the night of 14 March and all meals. Accommodation (bed and breakfast) for the night of 13 March preceding the Workshop will also be available at a cost of £30.

Participation in the Workshop is by position paper. Papers of *about 2-6 pages* addressing one or more of the topics above, or related issues, are invited.

5 Feb 1995	*Deadline for position papers*
10 Feb 1995	Notifications of acceptance and registration forms sent
21 Feb 1995	Booklet of position papers distributed

Please send position papers to PPECC

More Information

Membership is free, with applications welcomed at any time. For more information about this or any other aspect of the Community Club's activities please contact:

Mr. Brian Henderson
Secretary, PPECC
Tel.: 0235 446151
email: ppecc@inf.rl.ac.uk

WWW:
http://web.inf.rl.ac.uk/clubs/PPECC.html

APPENDIX 4.2B. WORKSHOP PROGRAMME

Tuesday 14 March 1995

1000 *Registration and Coffee*

1045 Chairman's Introduction
Peter Dew (University of Leeds)

1100 Invited Presentations

- 1100 A Parallel Computing Perspective
  Denis Nicole (University of Southampton)
- 1140 A Distributed Computing Perspective
  Gordon Blair (University of Lancaster)
- 1220 Languages, Libraries, Abstract Machines
  Tom Lake (InterGlossa Ltd, Reading)

1300 *Lunch*

1400 Selected Submitted Papers I

- 1400 A remote operations protocol used in a distributed parallel database
  Jeremy Carroll (Hewlett Packard)
- 1415 PVM and MPI applied to a master/slave parallel mesh generator
  N A Verhoeven, J Jones, N P Weatherill, K Morgan (Swansea)
- 1430 Parallelising CFD codes using PVM
  P W Grant, M F Webster, X Zhang (Swansea)
- 1445 Experience of Developing Codes for Distributed and Parallel Architectures
  S A Williams, G E Fagg (Reading)

1500 Introductions by Subgroup Chairmen

- 1500 Subgroup A: Compute intensive
  Nigel Weatherill (University of Wales, Swansea)
- 1520 Subgroup B: Data intensive
  Jon Kerridge (University of Sheffield)
- 1540 Subgroup C: Interaction/response intensive
  Roger Hubbold (University of Manchester)

1600 *Tea*

1620 Subgroups I: Discussions (in parallel)

1800 end Discussions

1930 *Workshop Dinner*

Wednesday 15 March 1995

0900 Portable Software Tools for Parallel Architectures
C P Wadsworth (RAL), C Barnes (EPSRC)

0920 Invited Presentation:

The BSP Approach to
Architecture Independent Parallel Programming
Bill McColl (University of Oxford)

1000 *Coffee*

1020 Subgroups II: Draw Conclusions (in parallel)

1115 Selected Submitted Papers II

- 1115 High level Sharing Through Abstract Data Types
  D M Goodeve, J M Davy, M Kara, P M Dew (Leeds)
- 1130 A BSP Approach to Discrete-Event Simulations
  R C Calinescu (Oxford)
- 1145 Discrete Event Simulation
  C J M Booth, J B G Roberts (DRA)
- 1200 Distributed vs Parallel: Comparing like with like?
  R J Loader (Reading)

1230 *Lunch*

1330 Subgroup Conclusions (Subgroup Chairmen)

1500 Discussion and Overall Conclusions (Chairman)

1530 *Tea and Depart*

APPENDIX 4.2C. WORKSHOP ATTENDEES

Dr David Al-Dabass	Nottingham Trent University	dad@doc.ntu.ac.uk
Miss C Barnes	EPSRC	SCBN0@ib.rl.ac.uk
Dr G S Blair	University of Lancaster	gordon@comp.lancs.ac.uk
Mr C J M Booth	DRA Malvern	cjmb@signal.dra.hmg.gb
Dr D R S Boyd	RAL	drsb@inf.rl.ac.uk
Mr R C Calinescu	University of Oxford	rcc@comlab.ox.ac.uk
Dr J J Carroll	Hewlett Packard Laboratories	jjc@hplb.hpl.hp.com
Mr C D Clack	University College London	clack@cs.ucl.ac.uk
Prof G Coulouris	Queen Mary & Westfield College	George.Coulouris@dcs.qmw.ac.uk
Prof D Crookes	Queen's University of Belfast	d.crookes@qub.ac.uk
Dr N Dakev	University of Sheffield	n.dakev@sheffield.ac.uk
Ms Monique Damitio	University of Exeter	monique@dcs.exeter.ac.uk
Prof P M Dew	University of Leeds	dew@scs.leeds.ac.uk
Dr Simon Dobson	RAL	sd@inf.rl.ac.uk
Mr G E Fagg	University of Reading	g.e.fagg@rdg.ac.uk
Mr Hugh Glaser	University of Southampton	hg@ecs.soton.ac.uk
Dr Ray Glover	Brunel University	raymond.glover@brunel.ac.uk
Dr D M Goodeve	University of Leeds	don@scs.leeds.ac.uk
Dr C Greenough	RAL	cg@inf.rl.ac.uk
Mrs K Haigh-Hutchinson	University of Bradford	k.haigh-hutchinson@bradford.ac.uk
Mr B W Henderson	RAL	bwh@inf.rl.ac.uk
Dr Roger Hubbold	University of Manchester	hubbold@cs.man.ac.uk
Mr D J Johnston	RAL	david@inf.rl.ac.uk
Mr Jason Jones	University of Wales, Swansea	cgjones@swansea.ac.uk
Dr Jon Kerridge	University of Sheffield	j.kerridge@dcs.sheffield.ac.uk
Dr Tim Kindberg	Queen Mary & Westfield College	T.Kindberg@dcs.qmw.ac.uk
Mr Simon Knee	Oxford University	simon.knee@prg.ox.ac.uk
Dr T W Lake	GLOSSA	Tom.Lake@glossa.co.uk
Dr Timothy Lanscar	BAe Airbus Limited	---
Mr David Lecomber	University of Oxford	david.lecomber@comlab.ox.ac.uk
Dr R J Loader	University of Reading	roger.loader@reading.ac.uk
Dr W F McColl	University of Oxford	wfm@comlab.ox.ac.uk
Dr V B Muchnick	University of Surrey	v.muchnick@ee.surrey.ac.uk
Dr D A Nicole	University of Southampton	dan@ecs.soton.ac.uk
Dr D P Rodohan	Brunel University	darren.rodohan@brunel.ac.uk
Dr N A Verhoeven	University of Wales, Swansea	n.a.verhoeven@swansea.ac.uk
Dr P J van Santen	Brunel University	peter.van.santen@brunel.ac.uk
Dr C P Wadsworth	RAL	cpw@inf.rl.ac.uk
Mr Yuyan Wang	University of Bath	cesyw@bath.ac.uk
Dr N P Weatherill	University College of Swansea	n.p.weatherill@vax.swansea.ac.uk
Mr K P Williams	University of Reading	k.p.williams@reading.ac.uk
Dr S A Williams	University of Reading	shirley.williams@reading.ac.uk
Dr S C Winter	University of Westminster	wintersc@westminster.ac.uk
Dr X M Zhang	University College of Wales	x.m.zhang@swansea.ac.uk

APPENDIX 4.2D. WORKSHOP ARTICLE FOR ECN (appeared May 1995)

Distributed *and* Parallel

The distinct branches of Parallel Processing and Distributed Computing have many issues in common but are addressing different user communities. This was the conclusion of a workshop of researchers arranged by the Parallel Processing in Engineering Community Club (PPECC) to consider the question: "Distributed vs Parallel: convergence or divergence?".

A clear consensus was that emerging operation systems based on microkernels, with multi-processor and multi-thread support, provide the key to future convergence in the technology base.

The PPECC Workshop brought together 45 active researchers, from both industry and academia, including technology specialists, applications developers, and engineering and other users. A booklet of 19 position papers submitted by attendees was distributed prior to the event. (A limited number of copies are available.)

The programme consisted of 4 invited keynote speakers, 9 selected position papers, and three subgroups to consider key aspects of the workshop theme.

The guest speakers provided a stimulating presentations detailing the current positions of research within the parallel and distributed sectors.

Denis Nicole (Southampton) discussed recent developments in parallel architectures and systems. These included fast, cheap microprocessors (providing virtually free computational power) and fast dedicated routers (providing communication power). Set against these are the delays in bringing products to market. System design and software construction are now major tasks crucial to future success but requiring significant time and effort. He observed that the distinction between distributed and parallel is about *trust* (is the other processor still there? will I mount his file system? can we share address spaces? etc) and outlined a spectrum of trust from a single operating system image to email composition/encryption.

Gordon Blair (Lancaster) discussed the trends in the distributed field, including: the use of microkernels, open distributed processing, the move to ATM networking, and distributed file systems. Arguments for and against convergence with the parallel field were summarised for each topic. The challenge for microkernels lay in lightweight threads and in supporting the network. Recent developments are moving to greater use of standards and open platforms to build operating systems themselves. Chorus is a typical system.

Tom Lake (InterGlossa) discussed recent developments within languages and libraries that provide support for both parallel and distributed programming. Many key ideas and philosophies used were originally developed in the 1960's. Modern-day software developments are now being supported by the use of a neutral intermediate language TDF and its parallel extension ParTDF.

Bill McColl (Oxford) discussed the Bulk Synchronous Parallel (BSP) approach to architecture independent algorithms across both parallel or distributed systems. This programming style allows the design and programming of algorithms using *barrier synchronisation* between *supersteps* and has a simple but powerful cost model based on four main parameters (p, s, l, g).

The three subgroups, with Chairmen as follows, considered the current provision against requirements from three perspectives:

* *Computationally intensive*
  Nigel Weatherill (Swansea)

* *Data intensive*
  Jon Kerridge (Sheffield)

* *Interaction/response intensive*
  Roger Hubbold (Manchester)

The first group reported that users and developers want access to well structured and sound programming design methodologies that encompass both parallel and distributed systems with smooth migration and scaling.

The second group reported that many users were now facing the management of large volumes of data. File systems were seen as a simple repository for storing data, but provide no effective data management support for accessing data. Database support was required to enable better data management to be incorporated into projects more easily, with parallel/distributed servers ready to fulfil future access requirements.

The third group reported that the distinctions between the two fields could be viewed as relating to two issues: performance (parallel) and reliability (distributed). Networked PCs were seen as the volume market for both communities.

One interesting view from the workshop was that many saw the operating system as an area where there was useful collaboration between the two communities. The Distributed Systems community took the approach of seeking to build from microkernels and open operating systems (such as Chorus), while the Parallel Processing community sought to construct communication harnesses/hardware that provided high-throughput.

In concluding, the workshop considered the future support needs of both user communities as the perceived convergence takes place. The key technologies in both fields need a wider dissemination as they are becoming more widely used across both areas.

It was felt that important topics for Training and Awareness activities include: "getting started", migrating between systems (including performance modelling), software availability (utilities and packages), SQL awareness and use (and support for moving to databases), and a seminar with a user focus on understanding the impact of parallel and distributed operating systems.

The participants enjoyed the bringing together of these communities and felt that further meetings and joint programmes should be encouraged.

A fuller report is in preparation and will be distributed automatically to those who attended the Workshop. Copies may also requested by contacting the PPECC Secretary (see **********).

Professor Peter Dew (Leeds)
Workshop Chairman

APPENDIX 4.3A/B/C. COURSE ANNOUNCEMENTS

The next 3 pages contain the announcement for the 3 courses developed:

4.3a *Parallel Fortran for Engineers* (repeated 14-15 June 1995)

4.3b *Parallel Processing Techniques*

4.3c *Parallel C for Engineers*

Engineering Applications IT Support ProgrammE (EASE)

Parallel Processing in Engineering Community Club

Parallel FORTRAN for Engineers

EASE Training Room & Classroom, Building R1, Rutherford Appleton Laboratory

Wednesday & Thursday, 13-14 July 1994

Engineers and scientists would love to run their FORTRAN applications on faster machines. However, access time to supercomputers such as the CRAY is limited and expensive. A new generation of high performance parallel architecture, based on microprocessors with high-speed interconnect, has the potential of providing an affordable desktop resource for compute intensive applications. This course will enable attendees to move their FORTRAN codes onto such systems:-

(1) by presenting material on the choices available,
(2) through practical "hands-on" work on a representative system

An important concern of the applications developer is standardisation.How can it be ensured that the work done today to run an application on a parallel system will still be valid in the future? The tutors will provide information on the standardisation efforts in progress and the best systems to support the portability and future-proofing of source code. The practicals are based on PVM 3 an up-to-date de-facto standard programming system portable between networks of UNIX workstations and dedicated parallel machines.

FORTRAN Products
- •Inmos FORTRAN
- •3L Parallel FORTRAN
- • i860 FORTRAN

Mechanisms
- •Language Extensions
- •Communication Libraries
- •Shared Memory Models

Parallelisation Techniques
- •Farming
- •Geometric Decomposition
- •Algorithmic Decomposition

Hardware
- • Plug-In Boards
- • Dedicated Parallel Machines
- • Providing a Networked Resource

Microprocessors
- •i860
- •C40
- •T800
- •T9000

Languages & Standardisation
- •FORTRAN 77
- •FORTRAN 90
- •High Performance Fortran (HPF)
- •Message-Passing Interface (MPI)

Timetable

Wednesday 13 July 1994

1000 *Registration and Coffee*
1030 Introduction and Overview
1130 Technical Presentations
1230 *Lunch*
1330 Practical Work
1515 *Tea*
1545 Practical Work
1700 *Close*

Thursday 14 July 1994

0930 Technical Presentations
1045 *Coffee*
1100 Technical Presentations
1230 *Lunch*
1330 Practical Work
1445 *Tea*
1515 Practical Work
1600 *Close*

Engineering Applications IT Support ProgrammE (EASE)
Parallel Processing in Engineering Community Club (PPECC)
Course

Parallel Processing Techniques

Tuesday & Wednesday, 25-26 October 1994
Rutherford Appleton Laboratory

The aim of this course is to teach a range of techniques for Parallel Processing and provide practical advice on when, where, why, and how to apply this knowledge. The intention is to take a higher level view of this rapidly changing field, and to arm you with general methodologies and principles that will stand the test of time whilst providing sufficient information to make effective use of current systems.

Although no single particular development system or implementation method will be addressed, a survey of those that are available will be provided, with worked examples being presented for a representative sample.

A detailed overview of the most commonly useful techniques and parallel programming styles will be presented on Day 1. Day 2 is oriented to implementation and performance issues, including advice on what to do if the performance of your parallel application falls short of what is expected. Real case studies will be presented, illustrating how to take an application right through to a parallel implementation. The focus of the applications and the case studies will be in the scientific and engineering domain. The teaching method is through lectures and class exercises in subgroups.

Who should attend?

- Researchers and developers expecting to use, or considering, parallel processing for their application
- Those already using parallel processing and seeking to broaden their knowledge of effective techniques and alternative approaches and systems
- Those seeking a strategic insight into where the field is going to safeguard their investment in parallel software development ("future proofing")
- Anyone wanting to find out more about parallel techniques

Prerequisites

- Familiarity with a programming language is assumed, though no particular one is necessary.
- Though the examples are from science/engineering, no specific knowledge is required from these fields.

Provisional Timetable

Day 1		Day 2	
10:00	*Registration and Coffee*	09:30	Factors Affecting Performance
10:30	Technological Background	10:00	Factors Controlling Performance
11:30	Parallel Paradigms	10:30	*Coffee*
12:30	*Lunch*	10:45	Exercises: Performance
13:30	Exercises: Parallel Paradigms	11:15	Trouble-Shooting
14:00	Programming Styles	11:45	Implementation Examples
15:00	*Tea*	12:45	*Lunch*
15:15	Programming Styles (continued)	13:30	Exercises: Realisation
16:00	Exercises: Programming Styles	14:30	*Tea*
17:00	*Close*	14:45	Cases Studies
		16:00	*Close*

Engineering Applications IT Support ProgrammE (EASE)
Parallel Processing in Engineering Community Club (PPECC)
Course

Parallel C for Engineers

Wednesday & Thursday, 18-19 January 1995
Rutherford Appleton Laboratory
EASE Training Room & Classroom, Building R1

Engineers and scientists would love to run their existing applications and those under development on faster machines. However, access time to supercomputers such as the CRAY is limited and expensive. A new generation of high performance parallel architecture, based on microprocessors with high-speed interconnect, has the potential of providing an affordable desktop resource for compute intensive applications. This course will enable attendees to move their C codes onto such systems, as well as develop parallel C codes from scratch. This will be achieved:-

(1) by presenting material on the choices available,
(2) through practical "hands-on" work on a representative system

An important concern of the applications developer is standardisation. How can it be ensured that the work done today to run an application on a parallel system will still be valid in the future? The tutors will provide information on the standardisation efforts in progress and the best systems to support the portability and future-proofing of source code. The practicals are based on an up-to-date *de facto* standard programming system portable between networks of UNIX workstations and dedicated parallel machines (one called the Parallel Virtual Machine (or PVM)).

Topics

C/C++
- C/C++ and Parallelism
- Parallel Libraries for Programmers
- C++ Class Libraries

Mechanisms
- Language Extensions
- Communication Libraries
- Shared Memory Models

Tools
- Automatic Parallelising Compilers
- Development Systems

Standards
- Message Passing Interface (MPI)
- Parallel Virtual Machine (PVM)
- P4

Parallel Techniques
- Message Passing Approach
- Shared Variable Approach

Parallelisation Techniques
- Farming
- Geometric Decomposition
- Algorithmic Decomposition

Timetable

Wednesday 18 January 1995

1000 *Registration*
1015 Introduction and Overview
1115 *Coffee*
1130 Technical Presentations
1230 *Lunch*
1330 Practical Work
1515 *Tea*
1545 Practical Work
1700 *Close*

Thursday 14 January 1995

0930 Technical Presentations
1045 *Coffee*
1100 Technical Presentations
1230 *Lunch*
1330 Practical Work
1445 *Tea*
1515 Practical Work
1600 *Close*

APPENDIX 4.6A/B. PUBLICITY LEAFLETS

The next four pages contain copies of

4.6a PPECC leaflet (2 pages)

4.6b PEC leaflet (2 pages)

Access Routes

The club provides a World-Wide Web access route to its events and activities. The service is accessed via the address:

http://web.inf.rl.ac.uk/clubs/PPECC.html

The club also maintains a maillist service on the national "mailbase" at Newcastle. The list "ppecc@mailbase.ac.uk" provides a forum for discussions and announcements by club members. To join this list server send a message structured:

> mail message

To:	mailbase@mailbase.ac.uk
Subject:	(you may leave this blank)
Text:	join ppecc Brian Henderson
	stop

replacing "Brian Henderson" with your forename/surname details.

Contact

Enquiries about the Community Club and its current activities can be directed to:-

B Henderson
ppecc@inf.rl.ac.uk
(Tel.: 0235-446151, Fax: 0235-445945)

Personnel

We have four specialists available to give advice and consultancy on parallel processing issues.

Dr. Chris Wadsworth: Parallel computing strategy, Programming methodologies, Portable parallel software, Parallelising serial software, Cost-effective parallel computing.

Dr. Simon Dobson: Parallel sharing, Novel languages, Small-scale parallelism, Windows NT.

Mr. David Johnston: Transputer systems, Transputer assembly language, Embedded Communication systems, Parallel Fortran.

Mr. Brian Henderson: Transputer systems, I860 & C40 Parastations, ANSI 'C', Parallel Fortran, Performance evaluation.

Membership

Membership if freely open to both Academics and Industrialists who have an interest in the application of parallel processing to engineering applications and problems.

If you would like to join the Community Club, or receive more information about the Centre facilities and other activities, please send an email message (strongly preferred) including your name, address, phone, fax and email details to ppecc@inf.rl.ac.uk or contact us directly.

PPECC

Parallel
Processing
in
Engineering
Community
Club

Objectives,
Facilities,
Contacts.

Background

* The PPECC was formed in 1993 after the successful examples of the Computational Fluid Dynamics Community Club (CFDCC) and Visualisation Community Club (VISCC) which are engendering cooperation and development in their particular fields.

* Support for PPECC is currently provided by the EASE programme, whose brief is to enhance the awareness and high quality application of IT in engineering research programmes.

* A Steering Group made up of researchers in both industry and academia has been formed to guide the activities of the club closely relating them to the need of the members.

Motivations

Parallel processing is a means to an end. Engineers, like other users, are typically motivated by its potential benefits:

* to run existing applications *cheaper*

* to run existing applications *faster*

* to tackle *bigger* problems

* to add more *functionality*

* to enable *new applications*

In short, better *performance* in one form or

Objectives of the Club

* to bring together researchers seeking to exploit the potential of parallel processing in their own areas of research.

* to provide a forum for the exchange of practical experience.

* to increase awareness of the benefits of parallel processing for engineering applications.

* to engender the development of cost effective solutions to engineering problems

* to encourage understanding, experimentation, and optimisation in the trade-offs between functionality, performance and cost.

Events

The club organises seminars, courses and workshop events to discuss and share experience of using parallel processing.

Seminar events provide particular focus on a single topic area, with speakers in that area highlighting current developments.

Courses provide distinct teaching of particular parallel skills and techniques.

Full details of the current event schedule of the club is available from the Club Secretary (see back page).

Facilities

The club maintains an equipment centre providing access to a range of affordable parallel hardware and software systems, much of this in the form of "add-ons" or "add-ins" to PCs or workstations.

Currently the Centre maintains a number of distributed memory systems:

4-node i860 Parastations,
2-node C40 Parastation,
24-node Parsys Supernode,
Various transputer installations.

and shared memory multiprocessors:

2-node Sun Sparc-10,
4-node 486-based PC.

Access is available to these systems to enable researchers to evaluate them against their requirements.

Other Initiatives

A parallel software archive is maintained by HENSA, the Higher Education National Software Archive. This archive can be accessed over internet using the address "unix.hensa.ac.uk". Access routes are supported using both FTP and WWW.

The parallel archive currently holds papers, codes and articles particularly focused on the Inmos Transputer and OCCAM language.

SYSTEMS

4-node I860(100Mz) Parastations.
2-node C40(50Mhz) Parastation.
24-node Parsys Supernode.
4-node AcerFrame 3000MP.
32-node Inmos ITEM-rack
Numerous TRAM products
Inmos B300 ethernet adapter.

SOFTWARE

3L : 'C', Fortran, Pascal
Inmos: ANSI 'C', VLC
PGI: Fortran, C
Parsys: Idris
GENYSIS
PVM
P4

FUTURE DEVELOPMENTS

The PEC forms a part of the programme Parallel Processing in Engineering Community Club (PPECC). The PEC provides equipment to members to evaluate their needs.

It is expected that Inmos T9000 based products will be added to the PEC once these products become generally available.

PERSONNEL

The PEC has four specialists available to give advice and consultancy on parallel processing issues.

Dr. Chris P Wadsworth: Parallel computing strategy, Programming methodologies, Portable parallel software, Parallelising serial software, Cost-effective parallel computing.

Dr. Simon A Dobson: Parallel sharing, Shared Objects, Small-scale Shared Memory systems, Windows NT, Transputers.

Mr. David J Johnston: Transputer systems, Transputer assembly language, Embedded Communication systems, Parallel Fortran.

Mr. Brian W Henderson: Transputer systems, I860 & C40 Parastations, ANSI 'C', Parallel Fortran, Performance evaluation.

ACCESS

Access to the equipment within the PEC is freely provided to grant-holding academics and PPECC members. Availablability to industrialists is by arrangement .

Enquiries can be directed to:-

B Henderson
ppecc@inf.rl.ac.uk
(Tel: 0235-446151, Fax: 0235-445945)

PARALLEL EVALUATION CENTRE

The Parallel Evaluation Centre (PEC), located at the Rutherford Appleton Laboratory, provides a range of affordable parallel hardware and software for academics and industrialists to test against their parallel processing requirements.

The PEC is located within the Informatics Department at RAL and operates using staff from the Parallel Processing Group. The PEC own a range of parallel processing facilities: including hardware based on current processors and various programming systems.

The processor types available within the PEC include:

- **Intel I860**
- **Texas Instruments C40**
- **Inmos T800 transputer Series**
- **Intel 486**

The programming methodologies supported by the PEC include:

- **Message Passing (MP)**
- **Shared Variables.**

This provides good coverage of the existing choices for researchers to choose from.

FACILITIES

TRANSPUTER SYSTEMS

The PEC maintains a large pool of transputer based systems ranging from single processor boards to a 24 node supercluster.

A Single board Transputer system can act as a simple accelerator device when attached to a PC. Increasing the number of boards gives rise to small-scale parallel systems that can be used to investigate basic parallel processing techniques.

Motherboards accommodating around 1-10 nodes provides mid-scale systems that can be added to a wide range of host systems: PC, Sun, HP, IBM RS/6000 etc. The motherboards take the INMOS TRAM modules that each incorporate a single transputer and associated memory.

A Parsys Supernode is available within the PEC. The supernode is a multi-node system which currently houses 24 T800 transputers. The system runs the Idris operating system which provides a UNIX-like programming environment. This system supports multi-user access to the available Transputers and dynamic reconfiguration of network topologies.

Finally a INMOS B300 is provided to enable transputer boards to be connected to the local Ethernet network with access available to other networks.

INTEL I860

We have two i860 based systems in the PEC. Both are Transtech Parastations which each house 4 compute nodes. Each Parastation is attached to a Sun workstation.

Each node in the Parastation consists of a 50Mhz i860XP (peak performance = 50MIPS, 100MFLOPS) and a 30Mhz T805 Transputer. A 4 node system provides peak power rating of 200MIPS and 400 MFLOPS.

The i860XP is a single chip microprocessor with on-board support for integer, floating point, graphic operations and memory management. The chip also contains a 16Kbyte instruction and data cache.

TEXAS INSTRUMENTS C40

Our C40 based system consists of a 2 node system, housed in a Transtech Parastation attached to a Sun workstation.

The C40(50Mhz) is a single chip microprocessor oriented to Digital Signal Processing (DSP). The chip has peak performances of 275 MOPS, 50 MFLOPS. The chip contains six 20Mbyte/s communication links to enable it to be constructed into network/parallel topologies.

MULTI-PROCESSOR PC

As well as the parallel systems constructed from specialist microprocessors we have also installed a parallel system based on the current industrial standard PC microprocessor the INTEL 486.

This is the ACER 3000-MP which provides 4 33Mhz 486 microprocessors with a single 32Mbytes of shared memory.

To capture the power of all 4 processors we run the new multi-tasking, multi-threaded operating system from Microsoft WINDOWS-NT.

This system can supports both investigations into shared memory systems and message passing systems.

WORKSTATION NETWORKS

An additional resource available to the PEC is a suite of 10 Sun SPARC_IPX workstations which form a training "set" for courses and seminars.

These workstations can be used to investigate software products such as PVM, P4 which link networked workstations into a single virtual distributed parallel machines.