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Silicon Tracker Data Acquisition

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ABSTRACT

Large particle physics experiments are making increasing technological demands on the design and implementation of real-time data acquisition systems. The LHC will have bunch crossing intervals of 25 nanoseconds and detectors, such as CMS, will contain over 10 million electronic channels. Readout systems will need to cope with 100 kHz rates of 1 MByte-sized events. Over 70% of this voluminous flow will stem from silicon tracker and MSGC devices. This paper describes the techniques currently being harnessed from ASIC devices through to modular microprocessor-based architectures around standards such as VMEbus and PCI. In particular, the experiences gained at the HERA H1 experiment are highlighted where many of the key technological concepts have already been implemented.

ACKNOWLEDGEMENT

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In particular the author wishes to acknowledge those made to the H1 Silicon DAQ system and the CMS Tracker Readout DAQ electronics by G.Noyes, R.Halsall and P.Burch of RAL Technology. This paper would not have been conclusive without their diligence in developing the various concepts into working, well-engineered, solutions. To this must be added the names of A.Campbell and S.Bourov who have laboured tirelessly at DESY to ensure a successful integration into H1.
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Many of the architectural ideas for the LHC systems continue to pour forth from S.Cittolin of CERN, Geneva.
Once again, appreciation goes out to the excellent cooperation of the companies involved in the development and implementation phases of the H1 system, notably Micro-Research of Helsinki and C.E.S. of Geneva.
Finally, the author is grateful for the support of the UK Particle Physics and Astronomy Research Council and the generous hospitality of the DESY and CERN laboratories.

INTRODUCTION

H1 is one of the experiments operating at the Hadron-Elektron Ring Anlage (HERA), a large particle physics proton-electron storage complex buried beneath the suburbs of Hamburg at DESY. A total of nearly one-half million analogue electronic channels are read out and digitised in tune with successive electron-proton bunch crossings of 96.064 nanoseconds. The early implementation of the data acquisition system has been described elsewhere [1,2]. Various levels of hardware triggering, software filtering and digital compression are employed in a real-time data acquisition environment consisting of several hundred processing elements embedded within the IEEE VMEbus standard [3]. The recent addition of silicon tracking devices [4] has prompted significant upgrades to its modular architecture, taking advantage of the technological trends since the system's first inception. As such it provides a significant pointer to the demands which will be placed on data acquisition and detector readout systems at the LHC.

Several large detector outlays are in the early stages of preparation for operation at the Large Hadron Collider (LHC), located at CERN, Geneva, by the year 2005. One of the experiments, CMS, will have over 10 million electronic channels providing a flood of information which needs to be synchronised with a 25 nanosecond bunch crossing period [5]. In a similar fashion to H1, several layers of sophisticated triggering, filtering and compression will be employed to reduce the final data throughput to reasonable mass-storage recording rates. The largest fraction (over 70%) will again originate from the tracking devices, in particular the silicon trackers and MicroStrip Gas Chambers (MSGCs).

Some key parameters of both systems are summarised in Table 1.

Parameter	***H1 1996***	***CMS 2005***
Bunch Crossing Interval	*96 ns*	*25 ns*
Level-1 Trigger Rate	*100 - 200 Hz*	*100 kHz*
Total Number of Electronics Channels	*≈ 500,000*	*≈ 15,000,000*
Average Total Event Size (formatted)	*100 kBytes*	*1 MByte*
Average Event Size from Tracking Detectors	*60 - 80 kBytes*	*700 kBytes*
Number of Readout Branch Units	*12*	*256 / 512*
Event Builder Bandwidth	*25 MBytes/sec*	*100 GBytes/sec*
Event Filter Computing Power	*1,500 MIPs*	*5,000,000 MIPs*
Data production	*≈ 10 GBytes/day*	*≈ TBytes/day*
Number of Readout/DAQ crates	*≈ 150*	*≈ 300*
Number of electronics boards	*≈ 2,000*	*≈ 5,000*
Total Cost DAQ + Readout Electronics	*≈ $15 M*	*≈ $100 M*

Table 1 : Breakdown of the H1 and CMS Data Acquisition Systems

Solid state devices are now commonly integrated into particle physics detectors to measure charged particle trajectories with the highest spatial resolution achievable [6,7]. At H1, silicon detectors are located inside the innermost jet chamber of the H1 central drift chamber tracking device within a 1.2 Tesla magnetic field. The Central Silicon Tracker (CST) provides high resolution tracking and vertex reconstruction in the central region, and the Backward Silicon Tracker (BST) extends this coverage to small backward angles. A beam pipe, with an inner radius of 35 mm, meets the additional need to shield the detector from synchrotron radiation.

H1 Central Silicon Tracker

The CST consists of two layers of double sided silicon strip detectors [8]. The inner layer (radius 50 mm) is a regular prism with 10 faces; the outer layer (radius 85 mm) is similar with 16 faces (Figure 1). Each face consists of six silicon detectors, of total length 360 mm, with readout at both ends. The strip pitch in ø is 25 μm and in z is 90 μm, offering an intrinsic resolution of 10 μm in R-ø and 20 μm in z. Resolutions of 15 μm and 25 μm, respectively, have already been achieved with the preliminary alignment of 1996.

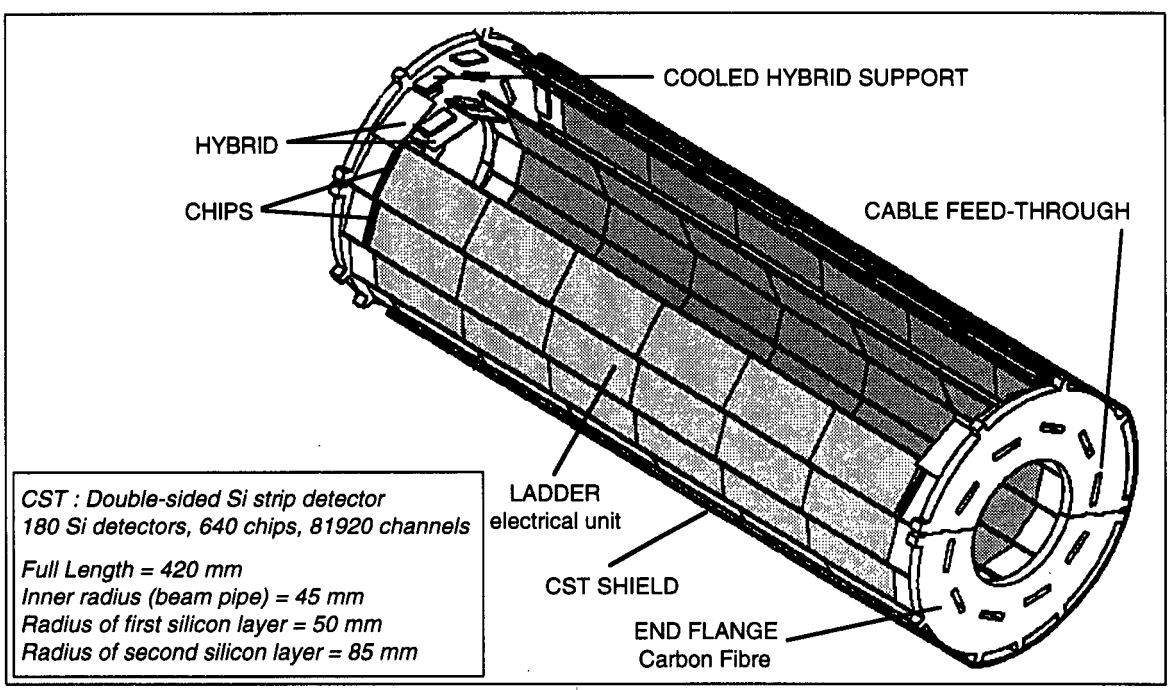

Figure 1 : H1 Central Silicon Tracker

H1 Backward Silicon Tracker

The BST consists of 8 planes of silicon detector discs (four in phase 1) mounted perpendicular to the beam line at distances between 280 mm and 860 mm from the nominal interaction point in the electron direction [9]. The discs have an inner hole of 55 mm radius and are segmented into 16 wedge-shaped, azimuthal sectors of four inch wafers with an outer radius of 125 mm (Figure 2).

Each disc is built as a composite of different silicon layers. One has a pad segmentation for triggering on deep inelastic electrons down to 1 GeV. The second layer has circular strips at constant radii (r-strips with a pitch of 48 μm) to measure the polar angle of backward scattered charged particles. The angular resolution of the r-strips is 0.5 mrad. A third layer, with strips at constant azimuthal angles (ø-strips with a pitch between 58 μm and 133 μm depending on the radius) to determine the transverse momentum of charged particles (resolution of 10% at 1 GeV/c, is also catered for.

As of publication, four planes are actively used in the detector with the remaining planes due later in 1997. The possibility of a similar device in the forward region is also foreseen. The CST is fully commissioned, with complete track reconstruction matched to the rest of the detector.

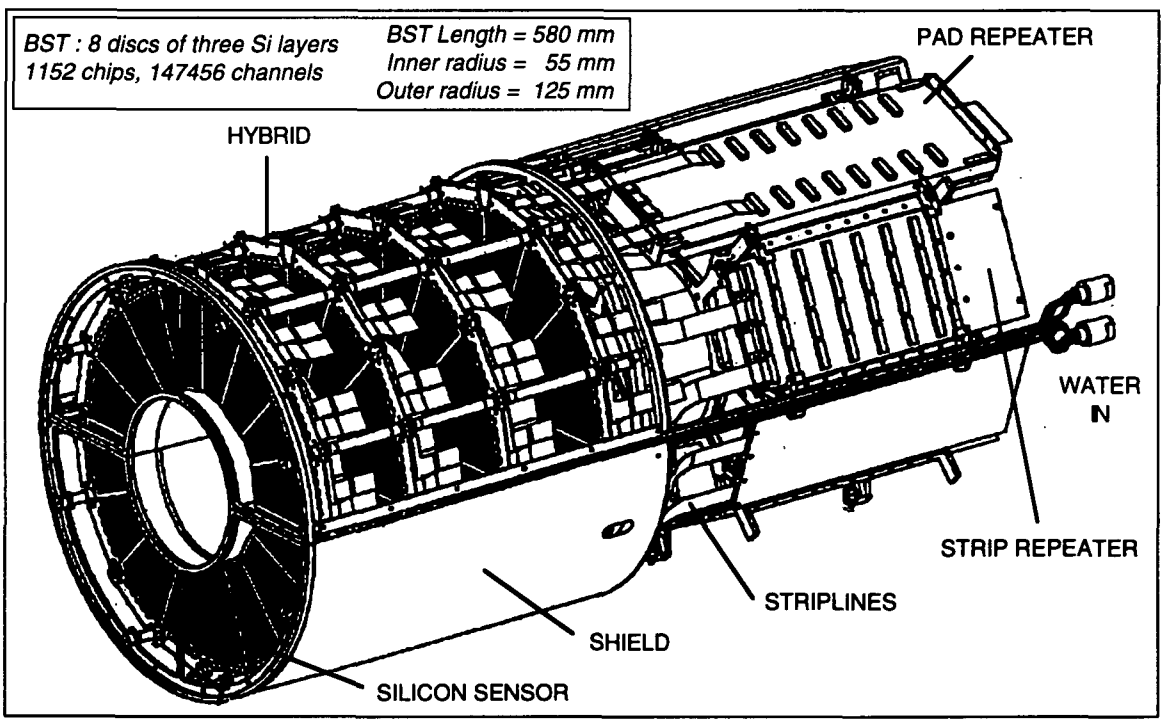

Figure 2 : H1 Backward Silicon Tracker; perspective of 4 planes and associated repeater electronics

Altogether there are 230,000 channels which are read out by custom-built chips and circuit VMEbus boards. A purpose-built "pipelined" triggering system (22 bunch-crossings long, dead-time free) is used to select initial candidates for data processing from the background of 10^4 events/s. A requirement on H1 is that, after an early level hardware triggering decision, all analogue signals should be read out within 800 μs.

The complete readout chain breaks down into the following 6 basic elements:
- the custom on-detector front-end chip (APC) to fulfill the requirement of a pipeline buffer to accommodate the HERA bunch repetition rate of 10.4 MHz,
- a decoder chip,
- a line-driver, for conventional copper cable or fibre-optics,
- a control module (OnSiRoC),
- a readout and processor module (PowerPC-ADC PMC)
- a master data acquisition controller (VMEtaxi).

The master controller supervises the readout and merges the data-stream into the VMEbus-based H1 data acquisition system via fibre-optic links.

H1 Amplifier Pipeline Chip, APC

The 230,000 electronic channels are read out by purpose-built front-end amplifier chips which contain switched capacitor analogue-pipeline buffers [10,11,12]. A single chip has 128 low-noise channels storing 32 consecutive bunch crossings. Pipeline control is synchronised to the 96 ns bunch crossing period. Thus the pipeline depth is well matched to the first level trigger decision time of 2.5 μs. The schematics of the front-end readout chip are shown in Figure 3.

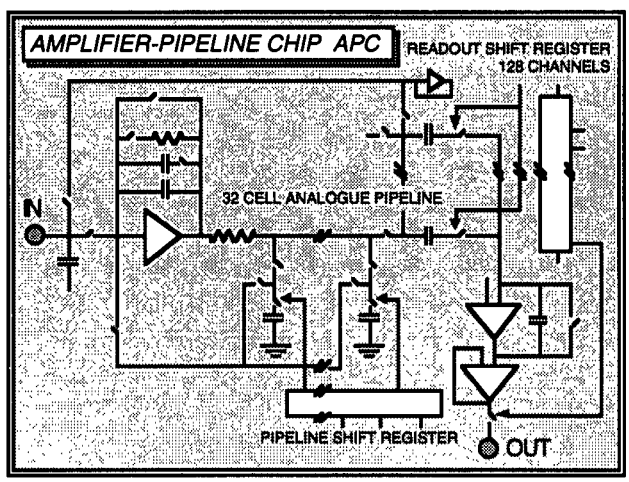

Figure 3 : H1 Amplifier-Pipeline Readout Chip

Each chip is fabricated in a 1 μm SACMOS (self-aligned CMOS) process with a 12.5 MHz switching rate and a readout speed of up to 4 MHz. This allows a 2000:1 multiplexing within the 800 μs readout time. The total power consumption of a single chip, including the pipeline running at 10 MHz, is less than 40 mW, whilst functionality with 2 μm CMOS prototypes has been maintained up to 100 krad (1 kGy) integrated dose from a Co^{60} source, the equivalent to 10 years of operation at H1; the SACMOS process further improves the radiation hardness and gives larger gain and improved stability. A signal to noise ratio of 14 has been achieved.

A total of 14 signals are necessary to control the pipeline and the shift register of the sequential readout. These signals are generated by a 'Decoder' chip which needs just 4 input lines. In both the 'sample' mode, when the information per 96 ns bunch crossing is stored into the pipeline capacitors, and in the 'readout' mode, when the information of a given time slice is read out sequentially at 2.5 MHz, the two phases of the clock are directly passed to the APC.

On-line Readout Controller

For APC control an external, custom-designed, VMEbus unit (OnSiRoC) is used [13,14]. Each module has a programmable sequencer unit for communication with the decoder chip and four independent sets each of three power supplies (strip detector bias voltage together with APC analogue and digital voltage).

The sequencer is used to store the intricate command sequences for controlling the APC. Sequences are arranged so that each sequence has a unique successor, with the possibility of endless loop command sequences interrupted by a trigger, e.g. when sampling. Thus, once the sequencer is loaded, a single command issued over the VMEbus can instigate the functional mode of operation on the APC.

H1 Silicon Tracker Data Acquisition

In order to realise fully the integration of the silicon tracker readout electronics into the H1 data acquisition, a coherent architecture has been established consistent with the rest of the system.

Overview of H1 Data Acquisition

The H1 data acquisition system consists of a modular multiprocessing environment designed around the IEEE VMEbus standard in the late eighties [1]. Several subdetector assemblies are read out in parallel by arrays of FADCs, DSPs and micros before being merged into a central coordinating framework. Altogether there are over 150 electronics crates. To avoid saturation on global VMEbusses, extensive use is made of the local VSB

specification [15]. To minimise any further potential dead-time losses, memory buffering is introduced at all key processing stages.

Currently events of size 100 kBytes can be coordinated with 12 branch-partitions at rates in excess of 100 Hz via a VMEtaxi dual optical fibre ring [16]. A parallel-filter farm of around 40 RISC processors (R3000 [17] and PowerPC [18]), with a performance equivalent of 70 IBM-3090 units in just 3 VMEbus crates, performs online reconstruction as well as providing a final level of full-event triggering [19]. The complete experiment is architectured so that graphics-orientated Macintosh stations provide a platform for both system operation and software development.

As such, the H1 system is capable of running entirely in VMEbus; dedicated processors executing dedicated tasks in real-time so that the net result is one of a conventional multi-tasking system. A well-defined, but essentially simple, framework is defined to enable external control and monitoring from commercially available computers and workstations. The graphics-based philosophy of these devices ensure that the operator is presented with, arguably, one of the most human-interactive interfaces to a complex real-time system.

ADC processing via PowerPC and PCI

The architecture of the silicon tracker readout follows that of the central data acquisition system by using fibre-optics and fast integer processing within a modular framework. Parasitic monitoring and reconstruction tasks can be executed in parallel using commercially available VMEbus RISC boards. Graphics-oriented workstations then cater for software development and operator-intervention. However it soon became apparent, during the first evaluation of the silicon devices, that a large amount of additional real-time processing capability would be required at the very front-end in order to deal with the intricate problem of hit-finding and pedestal calibration on an event by event basis.

Due to the huge strides consistently made in the microprocessor industry in recent years, in mid-1995 it became financially viable to develop a concept of large-scale ADC integration coupled closely with commercial processor cards to satisfy our requirements. In order to blend in homogeneously with the VMEbus environment, yet still provide enough bandwidth and buffering capacity to cater for the digital flow, the final ingredient was suitably provided by the PCI specification [20]. The advantages of adaptation are now well versed; PCI is now a popular standard within workstations, there is a defined PMC (PCI mezzanine) form factor adopted by all the major VMEbus producers, a planned evolution towards 66 MHz 64-bit and even an internal chassis definition of its own in Compact PCI.

As a consequence, it was decided to develop an ADC mezzanine in the double-sized PMC form factor and plug directly into the latest commercially available PowerPC [21] VMEbus cards, which also come equipped with up to 96 MBytes system memory [22]. The photograph, of Figure 4, shows a 100 MHz PowerPC 604 VMEbus card equipped with the RAL developed mezzanine for the H1 silicon readout. Each mezzanine contains 8 x 12-bit, 20 MHz ADCs [23]. Each ADC converts the analogue information from 16 amplifier pipeline chips. The output data from the ADCs are buffered into the local system memory of the PowerPC via PCI. The PowerPC executes data processing, hit-finding and pedestal monitoring together with the external system i-o communication to the rest of the DAQ.

The data are then read out over the 25 MBytes/s fibre-optic links of the VMEtaxi. Thus each PowerPC VMEbus board can handle 16,384 detector channels, allowing 1/4 million H1 silicon tracker channels to be read out and processed within one single 6U VMEbus crate.

The complete mezzanine readout system was designed, built and commissioned, with a full complement of system software, within less than a year. The initial idea was gelled during the summer of 1995, with approval and serious design work commencing that autumn. Already early in 1996 the first boards were fully tested in H1 yielding an effective resolution of 11-bits for the CST readout. By summer 1996 the full system was installed and operational. Half-way through the project the initial Chief Engineer departed for pastures new and yet, owing to the adoption of ISO9000 principles, his replacement was able to continue and still keep to schedule.

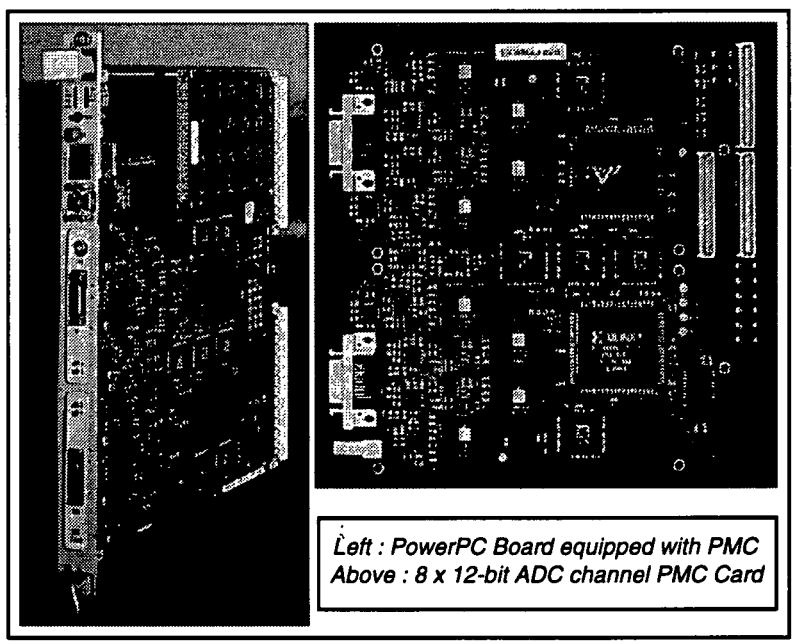

Figure 4 : PowerPC VMEbus board (CES RIO) and ADC PMC card

Integration into H1 Data Acquisition

The core of the silicon tracker readout is embedded into one VMEbus crate thanks to the compactness of the PMC solution and the benefits of modern IC integration. A VMEtaxi system then provides the overall coordination and interconnectivity.

VMEtaxi modules can connect VMEbus crates over several kilometres with multimode 100/140 µm, graded index, optic fibres [16,24]. Figure 5 illustrates the basic philosophy. The software protocol is purpose-written and optimised for speed and efficiency in a data acquisition environment [25]. There are many interesting analogies with the future international standard SCI [26]. During the early operation of H1, 25 MHz 68020 based boards were used with 125 MHz taxi chips. The upgraded "Mark-2" modules (VMExi2) are

able to exploit 50 MHz 68030 processors and 250 MHz taxi chips so that, by using double fibre-optic links in parallel, transfer rates of over 50 Mbytes/s are possible. The link reliability has been tested to a bit error rate of less than 1 in 10^{13}. Program memory is provided for by 128 kBytes of on-board dual-ported static ram, whereas EPROM and EEPROM cater for firmware storage and configuration parameters. In addition the on-board extension ram provides 2 MBytes of data memory. As a result the VMExi2 can be regarded as "3 boards in one" providing processing power, optic-fibre interconnectivity and data memory on a single-width VMEbus card.

The VMExi2 was commissioned into the H1 data acquisition system during the Spring of 1993, using 175 MHz taxi chips to achieve 33 MBytes/s peak transfer rates.

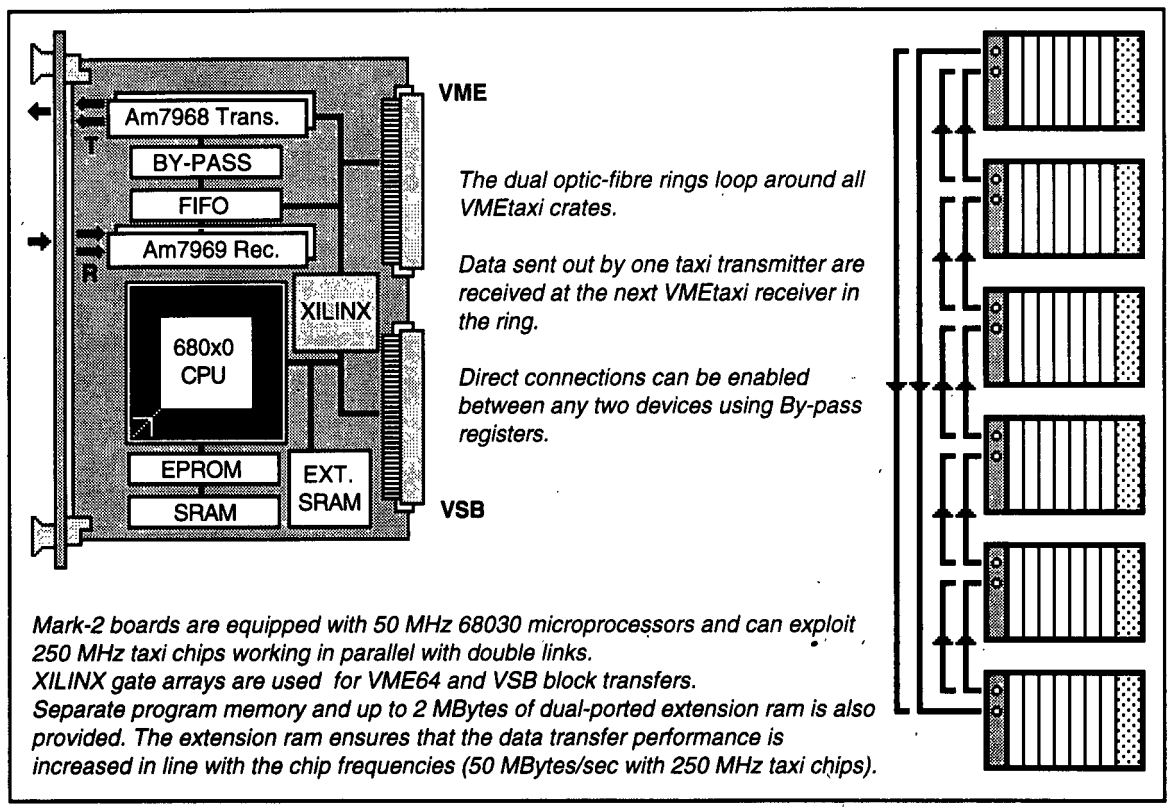

Figure 5 : VMEtaxi Mark-2

Further readout and reconstruction monitoring is carried out in a master monitoring crate by RISC-based cards similar to the filter-farm [27]. Memory boards provide the necessary buffers for readout and monitoring purposes [28]. In addition some 16 MBytes are required for the fast access of stored pedestal and sequencer RAM values together with readout configurations. Macintosh stations are employed to remain compatible with the rest of the H1 system for software development and operator control. One device is primarily responsible for the global operation of the data acquisition, a second provides event displays and histogram monitoring and a third takes care of the monitoring of slow control information using LabVIEW [29,30,31]. Macintosh personal computer access is through MacVEE [32,33,34] or, if 32-bit access is required, through MAC 7212 [35]. Existing software development tools [36] and techniques [37] as used in the rest of the data acquisition system

are exploited. Data quality can be monitored via event displays and histograms of, for example, pedestal and noise values, signal to noise ratios, clusters, radiation ageing (via the APC), etc., all with purpose-written programs layered on top of the existing base software packages of the H1 data acquisition system. Much of the binning and monitoring is carried out in dedicated tasks which execute permanently within the cost-effective VMEbus processors, thereby leaving the Macintosh as the graphical user interface. Such a solution has the added advantage that the VMEbus part runs as a self-contained entity, according to the protocol of the complete experiment, and is able to update the monitoring data sent to the rest of the acquisition system independent of the functionality of a local interface station. Finally a Subsystem Trigger Control Crate handles the H1 triggering protocol [38].

H1 Silicon Tracker DAQ Software

There is a well-ordered structure defined by the modular architecture of the hardware which defines how the software is written and developed. Dedicated tasks run on dedicated processors throughout the VMEbus system with operator intervention provided for via graphics-orientated workstations [39,40]. Devices such as the Macintosh provide a convenient integral component in both software development and operator-control. In order to embrace the framework of VMEbus, extra tools have been developed to ease the integration into the VMEbus [36] and exhaustive software libraries cater for external control by providing a full set of routines for system configuration, testing, system-status and monitoring [25,37,41,42]. These are based on relatively simple memory-mapped mailbox concepts for inter-processor communication (command blocks with arguments) and a well layered modularity which clearly separates the different levels, such as the dedicated package written for the VMEtaxi (Figure 6). The object-orientated world of the workstation thus becomes disentangled from the complex firmware code executing on the hardware except at clean and well-defined boundaries.

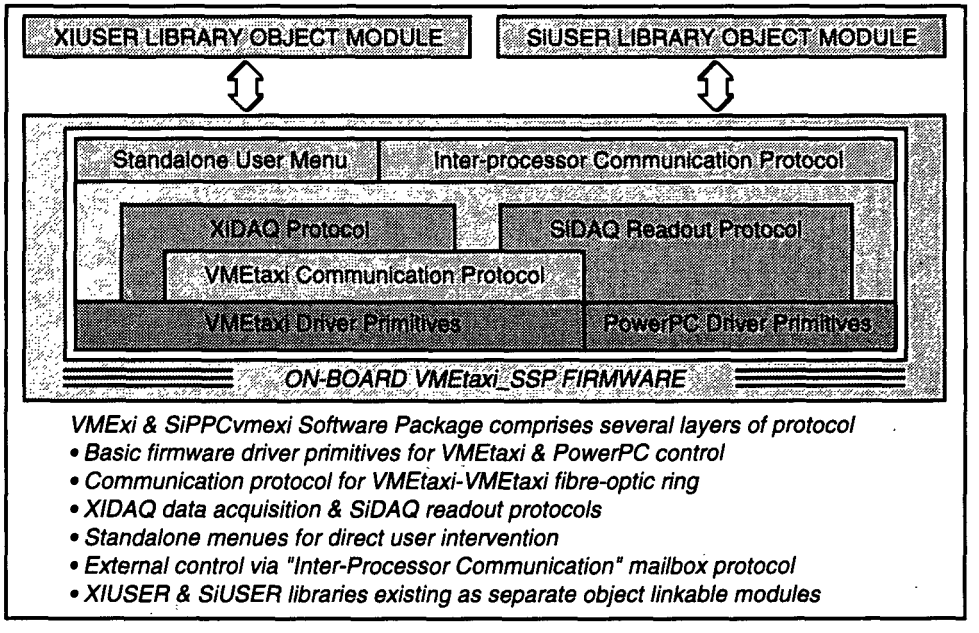

Figure 6 : Software Structure of the SiPPCvmexi package

For the development of flexible algorithms which need to be embedded into the firmware task, external hooks are provided for within the firmware code itself, e.g. for hit detection. These algorithms (as with the object-orientated workstation modules) can be developed platform independent in the high-level environment of choice. The resulting object modules can then be loaded and stored in battery backed-up memory. Upon the next system reset, the firmware task automatically re-loads and links the module into its system memory and calls appropriately [41,43].

Such an approach dispenses with the need for a potentially performance depriving operating system executing on the VMEbus processors at the heart of the system. Moreover, the discipline imposed lends itself to the ever changing world of platform independence. What is desirable is a standard debugging environment which could be agreed upon by industry. Nevertheless, particle physics data acquisition systems, despite their size, blend to the simplest form of multiprocessing software by placing independent programs on multiple CPUs with a relatively basic communication protocol between them.

THE CMS CENTRAL TRACKING SYSTEM

Silicon tracking devices form only a part of the H1 tracking capability. A large volume of the detector consists of conventional drift chambers. Such a design is not possible in the case of LHC. In order to deal with the large track multiplicities at CMS, detectors with small cell sizes will be mandatory.

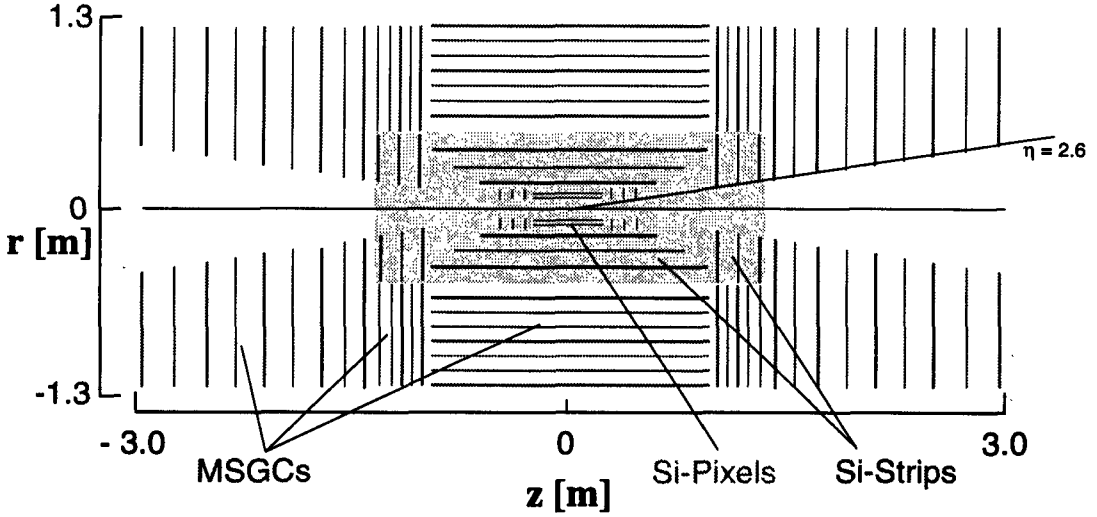

Figure 7 : Schematic of the CMS inner tracker. Thick lines denote double-sided readout.

Near to the interaction vertex there are planned to be several layers of silicon pixel detectors to provide space point measurements and improve secondary vertex detection. At larger distances from the interaction region silicon microstrip and gas microstrip detectors

are foreseen with strip-lengths/pitch of 12.5 cm/50 μm and (12.5 or 25) cm/200 μm respectively. In total, on CMS, the tracking volume is cylindrical with a length of 7 m and a diameter of 2.6 m (Figure 7). Together with a high magnetic field of 4 Tesla, the goal is to achieve a momentum precision of $\Delta p/p \approx 0.15 p_T$ (p_T in TeV) for all high p_T muons and isolated electrons produced in the central rapidity region.

CMS Tracker Readout Overview

The inner CMS tracking subdetectors will total some 12 million electronics channels from the MSGCs (8 million) and silicon strips (4 million). With an anticipated occupancy of 3 % this will still contribute around 700 kBytes of digitised information to final event sizes at the 100 kHz Level-1 trigger rate. Figure 8 presents a schematic overview of the readout chain, having been extensively reviewed elsewhere [44,45].

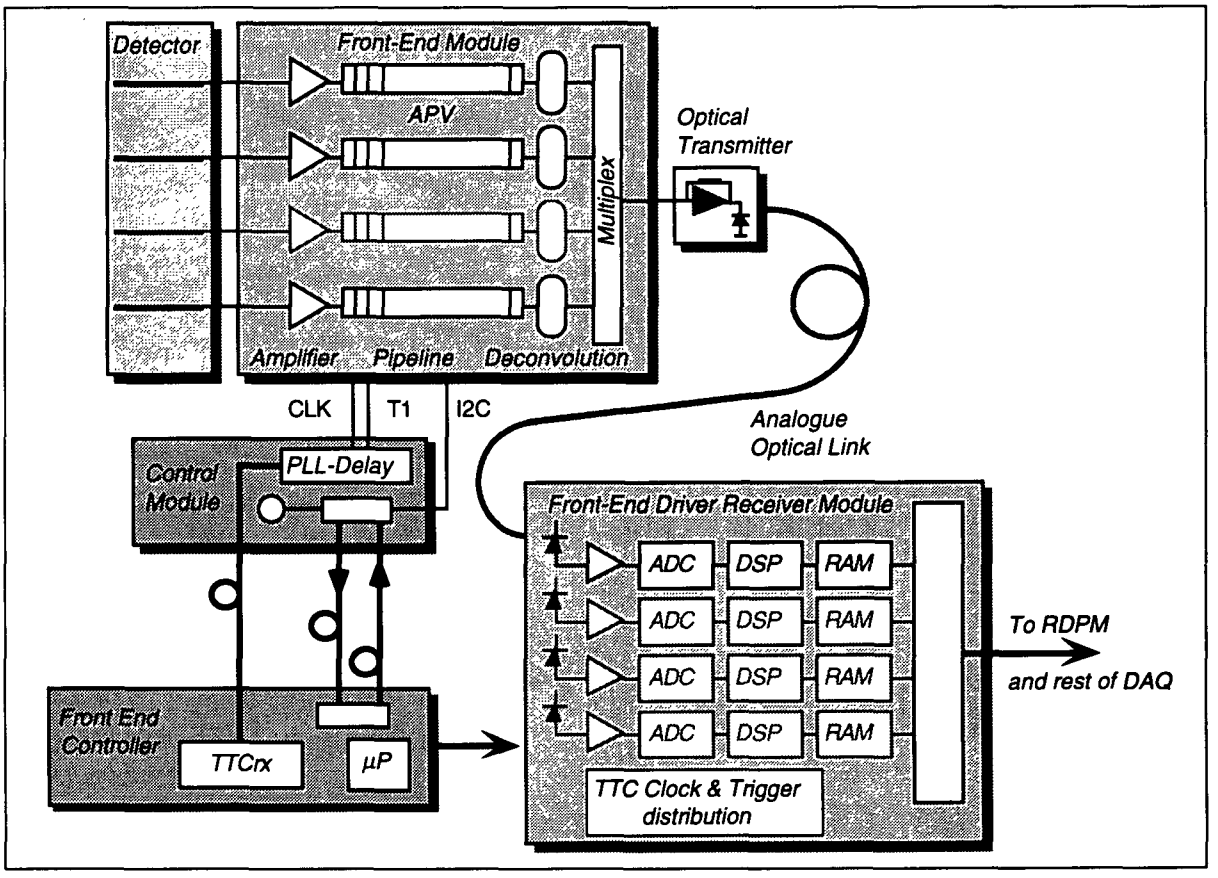

Figure 8 : Overview of the front-end of the CMS tracker electronic readout chain

Each microstrip is read out by a charge sensitive amplifier with a 50 ns time constant whose output voltage is sampled at the 40 MHz bunch-crossing rate within an APV6 chip [46,47,48]. Each chip can read out 128 channels and has a pipeline depth for up to 128 crossings (3.2 μs). Its novel feature is the use of analogue deconvolution of the shaped and amplified signal pulse to give the precise timing information required at LHC for fast signals from silicon detectors. The Harris 1.2μm AVLSIRA CMOS version of the chip has an

area of 6.4mm x 11.2mm with a maximum power budget of 2 mW/channel, being radiation-hard up to 10 Mrad [49]. It is likely that up to half the number of chips required could also be fabricated in the DMILL process [50].

The digital conversion and readout processing will be based in VMEbus, similar to H1, and sited some distance away from the on-detector APV chips. Therefore it is intended that the pulse height data from each channel will be serially transferred at 40 MHz, without zero suppression, by a fibre-optic link to a Front-End Driver receiver module using a multiplexing level of 256 detector channels per fibre (two APVs being multiplexed via an APVMUX chip). Since each analogue value corresponds to 6-8 bits of information, the effective equivalent digital transmission rate is some 80 Gbit/s [51,52,53]. The Front End Driver, discussed further below, digitises the analogue data, performing zero suppression and simple cluster finding, before storing the results in a local memory analogous to the PowerPC-PMC board on H1 [54]. At CMS, a separate Front End Controller (FEC) will be responsible for control of the front-end chips via separate fibres (but same technology as the analogue transfer) in a similar fashion to the H1 OnSiRoC [55]. The CMS FEC will also distribute the LHC clock and trigger signals via the CERN developed TTC system [56,57].

Again, the main reasons for adopting the analogue solution is the improved position resolution at small angles and the immunity to unexpected noise, allowing any corrections to be applied off-detector. Moreover, the ready access to external "bulk" electronics off-detector is more than attractive from the maintenance and replacement point of view. Of course the costs have to be balanced, but again the commercial availability of FADCs is far more economic than the implementation of customised radiation hard componentry.

CMS Data Acquisition Overview

Before discussing the Front-End Driver it is necessary to consider its function in relation to the rest of the CMS data acquisition system. Indeed, as already indicated, the largest contribution to the data flow arises from the inner tracking detectors so that, in the end, the DAQ system has to merge 1 MByte of formatted events from the many front-end sources at Level-1 trigger rates up to 100 kHz.

A more complete description of the CMS Data Acquisition system is given in chapter 9 of the technical proposal [5]. Given the high Level-1 trigger rate, the total event size which has to be merged and the capabilities of mass storage media, technology and logistics dictate that many individual sources of data need to be buffered deep enough while a sophisticated filtering decision is performed. At present, it is anticipated that a high performance readout network will connect the various sub-detector readout elements via a switch fabric to a computer farm performing this high-level filtering. From the viewpoint of the front-end, the connection to this network will need to be via a fast, and deep, dual-ported memory.

The basic unit which connects the CMS front-end subsystems with the rest of the data acquisition is termed a Readout Unit. Each Readout Unit consists of a Front-End Driver (FED) and a fast Readout Dual-Port Memory (RDPM) [58] which, in turn, is connected to the global event-building switch fabric. With approximately 500 such units, each RDPM must be capable of buffering up to 100,000 event fragments, namely 200 MBytes, and of

performing data transfers up to 400 MByte/s on both input (from the FED) and output (to the switch) ports. Each RDPM is attached to between one and six FEDs, depending on the local event data volume and the event builder switch input rate. Physically, a readout crate will contain several Readout Units together with a crate controller and communication module. The dual functionality of both the controller/communication module and the RDPM is analogous to the role of the VMEtaxi on H1.

Nearly 1,500 FEDs will be necessary for the whole detector; around half of which are required for the tracking. It is clear that, though there are several different subdetectors other than the tracker, the standardisation of a common electronics interface at this junction will ensure system homogeneity, simplifying integration and long-term maintenance tasks.

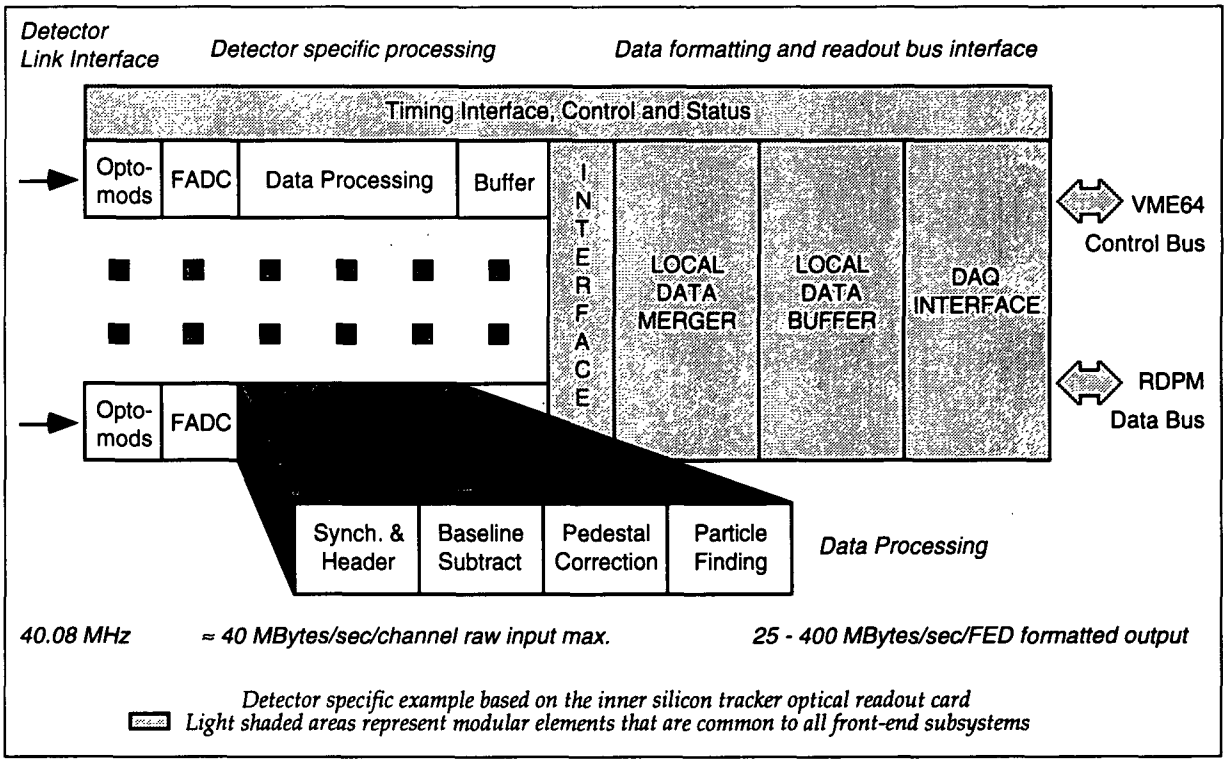

Figure 9 : Key elements of the CMS Tracker Front-End Driver

CMS Tracker Front-End Driver

The requirements of the CMS Tracker Front-End Driver (FED) are thus, primarily, two-fold. First, it must accommodate the detector dependent functionality of the very front-end electronics. Physically 256 detector channels are multiplexed onto one fibre which must be received by an 8-bit, 40 MHz ADC. Up to 64 ADC channels are foreseen on one 9U FED. Thus a total of around 750 Tracker FEDs are envisaged presently to read out the whole of the CMS tracking alone. Second, the FED must be able to deliver its output to the data acquisition, specifically the RDPM, at rates up to 400 MBytes/s. Since much of the logic must address the problems of pre-buffering, local data merging and error recovery as well as the fast RDPM interconnection, this second part is best designed in common with all the subdetector front-end subsystems [59].

Figure 9 shows a general overview of the functionality of the CMS Tracker FED card. Much of the board area is devoted to detector specific functions, such as digitisation and data processing, but a significant fraction of the logic is dedicated to the local merging of information, such as bunch numbers delivered by the TTC receivers, and to the fast links with the RDPM. Each FED has two access ports. A standard VMEbus interface provides overall control and monitoring in addition to the dedicated RDPM link for data throughput.

A prototype FED has already been built and beam tested at CERN with a detector module [60,61]. The primary aim of the prototype Front End Driver, shown in Figure 10, was to demonstrate the technical feasibility of building a high density (64 channel) FED in a large format module (9U x 400 mm). Achieving this high channel density per module is a key factor in demonstrating that the analogue receiver system can occupy a reasonable physical space. Other key factors are cost, power, analogue signal integrity, ADC resolution, digital signal processing, DAQ interface, data bandwidths & trigger rate. The module can also be used as an experimental vehicle to allow the engineering and detector teams to investigate technologies and techniques as part of the evolution towards the final design. In addition it can be used to test the basic functionality of the RDPM over the VMEbus port.

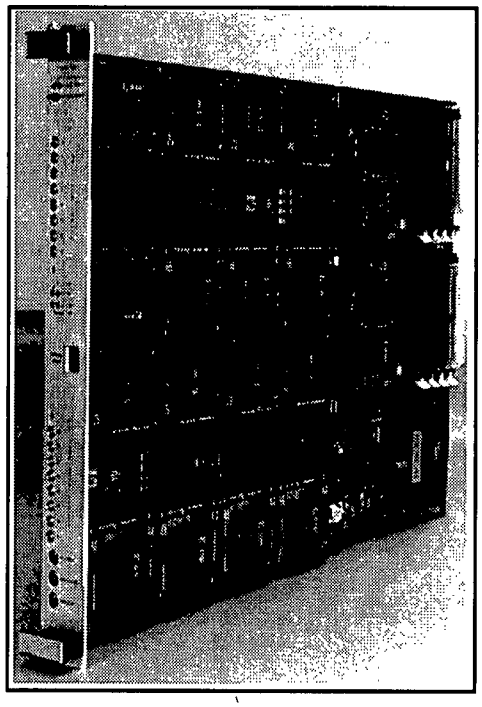

Figure 10 : Prototype Front-End Driver for first tests of the CMS Tracker

However, as a result of the experience gained with H1, and with a view to testing the feasible functionality of the RDPM over an input port other than VMEbus, the next stage of CMS FED development will involve designs around the PCI concept. Presently an 8-channel ADC, 40 MHz, single PMC form factor is under design with a view to being mounted on both a custom 9U-based motherboard and also commercial 6U VMEbus cards similar to H1 [62]. The beauty that such a PMC could also be used to test smaller prototype

detectors direct from PCI-based workstations, or within a Compact-PCI chassis, is also a compelling factor. Furthermore, it could well lead to a re-appraisal of what to accommodate on additional FED PMCs in view of the common functionality requirement across all subsystems.

OBSERVATIONS AND FUTURE PERSPECTIVES

The impact of the mid-nineties style technological approach is immediately visual when one sees the existing H1 system in action. The number of channels being read out from the silicon trackers alone is similar to that from the rest of the detector. Whereas the rest of the detector needs over 100 crates of digitising electronics, largely designed in the eighties, to assimilate its information flow, the whole silicon readout system is contained, essentially, in one double-height Euro-sized (6U) VMEbus crate. With the advent of faster modular-based busses such as PCI and the increasing trend of ever more transistorised componentry at the chip level, the stage is set to re-assess our architectural baselines in data acquisition design. By viewing our modularity around interchangeable PMC-like form factors, and marrying commercial with in-house custom solutions, the challenge presented by enterprises such as LHC become a lot more comprehensible and achievable. Indeed, even in the shorter term, consideration is being given to the adoption of PMC principles in other areas of the H1 system to add more flexibility for planned HERA luminosity increases from the year 2000, including PCI-based interconnectivity between front-end crates and workstations [63,64].

The price-performance improvements of microprocessor technology seem to continue unabated. It is likely that in the future, faster microprocessor implementations with increasing memory chip densities will be commercially available on such small, interchangeable, form factors. In the world of fast data movement, this could well prove fundamental towards harnessing the process of full event data merging given the relatively modest advances in the telecommunications and mass-storage industry in comparison.

CONCLUSION

Tracking devices have long been a major factor to the problem of data acquisition in large particle physics experiments. The demands placed on data throughput and processing have to be matched with autonomy, flexibility, upgradability and modularity coupled with longer-term durability. With shrewd design, around modern bus-based architectural concepts, even the future challenges can be met by taking advantage of the rapid rate of technological advances, particularly in chip component densities. Indeed, it is tempting to speculate that as microprocessing capability further evolves, the subtleties of system design will be even more focussed around intricate and innovative solutions at the readout level rather than at the later stages of data acquisition handling.

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