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Luigi Gaioni, on behalf of the RD53 Collaboration

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Test results and prospects for RD53A, a large scale 65 nm CMOS chip for pixel readout at the HL-LHC

Luigi Gaioni*

on behalf of the RD53 Collaboration[1]

Abstract

The CERN RD53 collaboration was founded to tackle the extraordinary challenges associated with the design of pixel readout chips for the innermost layers of particle trackers at future high energy physics experiments. Around 20 institutions are involved in the collaboration, which has the support of both ATLAS and CMS experiments. The goals of the collaboration include the comprehensive understanding of radiation effects in the 65 nm technology, the development of tools and methodology to efficiently design large complex mixed signal chips and, ultimately, the development of a full size readout chip featuring a 400×400 pixel array with 50 μm pitch. In August 2017, the collaboration submitted the large scale chip RD53A, integrating a matrix of 400×192 pixels and embodying three different analog front-end designs. This work discusses the characteristic of the RD53A chip, with some emphasis on the analog processors, and presents the first test results on the pixel array.

1. Introduction

Very high particle rates and radiation levels will be reached in the so-called Phase II upgrades of the ATLAS and CMS experiments at the High-Luminosity (HL) Large Hadron Collider (LHC). the HL-LHC will be delivering a huge amount of data during its operation, resulting in a set of demanding specifica-

*Corresponding author, email address: luigi.gaioni@unibg.it

[1]The RD53 Collaboration: [a]M.B.Barbero [a]D.Fougeron [a]S.Godiot [a]M.Menouni [a]P.Pangaud [a]A.Rozanov [a]P.Breugnon [b]M.Bomben [b]G.Calderini [b]F.Crescioli [b]O.Le Dortz [b]G.Marchiori [c]D.Dzahini [c]F.E.Rarbi [d]R.Gaglione [e]H.Krüger [e]M.Daas [e]Y.Dieter [e]T.Hemperek [e]F.Hügging [e]K.Moustakas [e]D.Pohl [e]P.Rymaszewski [e]M.Standke [e]M.Vogt [e]T.Wang [e]N.Wermes [f]M.Karagounis [f]A.Stiller [g]C.Marzocca [h]G.De Robertis [h]F.Loddo [h]F.Licciulli [i]A.Andreazza [i]V.Liberali [i]A.Stabile [i]L.Frontini [j]M.Bagatin [j]D.Bisello [j]S.Gerardin [j]S.Mattiazzo [j]A.Paccagnella [j]D.Vogrig [j]S.Bonaldo [k]N.Bacchetta [l]L.Gaioni [l]F.De Canio [l]M.Manghisoni [l]V.Re [l]E.Riceputi [l]G.Traversi [m] L.Ratti [m] C.Vacchi [n]K.Androsov [o]R.Beccherle [o]G.Magazzu [o]M.Minuti [o]F.Morsani [o]F.Palla [o] S.Poulios [p]G.M.Bilei [p] M.Menichelli [q] S.Marconi [q] P.Placidi [r]G.Dellacasa [r]N.Demaria [r] G.Mazza [r]E.Monteil [r]L.Pacher [s]A.Paternò [r] A.Rivetti [r] M.D.Da Rocha Rolo [t]D. Gajanana [t]V.Gromov [t]B.van Eijk [t]R.Kluit [t] A.Vitkovskiy [u]T.Benka [u]M.Havranek [u] Z.Janoska [u]M.Marcisovsky [u] G.Neue [u]L.Tomasek [v]V.Kafka [v]V.Vrba [w]E.Lopez-Morillo [w]F.R.Palomo [w]F.Muñoz [x]I.Vila [x]E.M.S.Jiménez [y]D.Abbaneo [y]J.Christiansen [y]S.Orfanelli [y]L.M.Jara Casas [y]E.Conti [z]S.Bell [z]M.L.Prydderch [z] S.Thomas [z1]D.C.Christian [z1]G.Deptuch [z1]F.Fahim [z1]J.Hoff [z1]R.Lipton [z1]T.Liu [z1]T.Zimmerman [z1]S.Miryala [z2]M.Garcia-Sciveres [z2]D.Gnani [z2]A.Krieger [z2]K.Papadopoulou [z2]T.Heim [z2]R.Carney [z2]B.Nachman [z2]C.Renteira [z2]V.Wallangen [z3]M.Hoeferkamp [z3] S.Seidel

[a]Aix Marseille Université, CNRS/IN2P3, CPPM, Marseille, France [b]Laboratoire de Physique Nucléaire et de Hautes Energies (LPNHE) Paris, France [c]Laboratoire de Physique Subatomique et de Cosmologie (LPSC), Grenoble, France [d]Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP), Annecy-le-Vieux, France [e]Rheinische Friedrich-Wilhelms-Universität Bonn Physikalisches Institut, Bonn, Germany [f]Fachhochschule Dortmund, Germany [g]Politecnico di Bari, Bari, Italy [h]INFN Sezione di Bari, Bari, Italy [i]INFN Sezione di Milano and Università degli Studi di Milano, Milano, Italy [j]INFN Sezione di Padova and Università di Padova, Padova, Italy [k]INFN Sezione di Padova, Padova, Italy [l]INFN Sezione di Pavia and Università di Bergamo, Bergamo, Italy [m]INFN Sezione di Pavia and Università di Pavia, Pavia, Italy [o]INFN Sezione di Pisa, Pisa, Italy [n]INFN Pisa and Università di Siena, Siena, Italy [p]INFN Sezione di Perugia, Perugia, Italy [q]INFN Sezione di Perugia and Department of Engineering, Università di Perugia, Italy [r]INFN Sezione di Torino, Torino, Italy [s]INFN Sezione di Torino and Politecnico of Torino, Torino, Italy [t]National Institute for Subatomic Physics (NIKHEF), Amsterdam Netherlands [u]Faculty of Nuclear Sciences and Physical Engineering of the Czech Technical University (FNSPE-CTU) [v]Institute of Physics of the Academy of Sciences of the Czech Republic (IP-ASCR) [x]Instituto de Fisica de Cantabria (IFCA, CSIC-UC), Santander, Spain [w]Electronic Engineering Dept, School of Engineering, Sevilla University, Spain [y]European Organization for Nuclear Research (CERN), Geneva, Switzerland [z]Science and Technology Facilities Council, Rutherford Appleton Laboratory, Chilton, Didcot, United Kingdom [z1]Fermi National Accelerator Laboratory (FNAL) Batavia, USA [z2]Lawrence Berkeley National Laboratory (LBNL), Berkeley, USA [z3]University of New Mexico (UNM), Albuquerque, USA

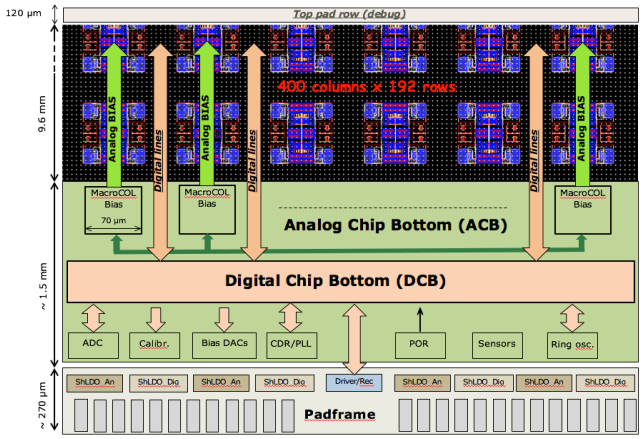

Figure 1: Functional view of the RD53A pixel chip.

tions for the detectors closest to the collision region, concerning both sensors and readout chips. The front-end electronics will be required to provide robust operation in a harsh radiation environment, with an estimated total ionizing dose (TID) of 1 Grad and 1 MeV neutron equivalent fluence of 2×10^{16}cm^{-2} accumulated during their lifetime, and hit rates of the order of 3 GHz/cm^2. Target pixel size will be 50 μm $\times$ 50 μm for the innermost layer of the tracker, with a power budget close to 0.5 W/cm^2, needed to keep the material budget and the complexity of the cooling system at a minimum. In order not to degrade detection efficiency, operation of the readout channel at low thresholds, around 1000 electrons or lower, has to be envisaged, setting challenging requirements on noise and threshold dispersion performance.

The design of an advanced pixel readout chip, called RD53A, has been tackled in a 65 nm CMOS technology in the framework of the RD53 collaboration [1], in view of the development of the production chip for the ATLAS and CMS experiments upgrades at the HL-LHC. The 65 nm technology, whose radiation tolerance properties have been thoroughly investigated in RD53, both for analog and digital circuits [2], enables the integration of dense in-pixel digital functions, needed to comply with the bandwidth requirements set by the high rates foreseen in the experiments.

The main goals of the RD53 collaboration include the detailed understanding of radiation effects in the 65 nm CMOS technology, the development of tools and methodology to efficiently design large, complex mixed-signal chips and, ultimately, the design and characterization of a full sized pixel array chip.

2. The large scale chip RD53A

The RD53A chip includes a 400 $\times$ 192 pixel matrix with 50 μm $\times$ 50 μm pitch and size of 20.0 mm $\times$ 11.5 mm, and will serve the purpose of qualifying the 65 nm technology for the development of the production chip. RD53A integrates three versions of analog front ends, called Synchronous, Linear and Differential. 128 columns are allocated for the first one, and 136 for each of the remaining ones, resulting in three different sub-matrices, featuring 192 rows, whose performance can be thoroughly assessed and compared. All the three analog front-ends implement a Time-over-Threshold (ToT) technique to perform analog-to-digital conversion, and share other constraints and features, such as the layout area and the bump bond pads, making them easily interchangeable on the pixel matrix. The basic analog front-end building block is referred to as a quad, and features a layout area of 70 μm $\times$ 70 μm, integrating four front-ends and four bump pads on a 50 μm $\times$ 50 μm grid. As far as the digital readout is concerned, RD53A embodies two different architectures, called Distributed Buffering Architecture (DBA), adopted for the Linear and the Differential front-ends, and Centralized Buffering Architecture (CBA), exploited for the Synchronous front-end. These architectures explore two different solutions which allow the sharing of the buffering resources in the limited pixel area.

As shown in Fig. 1, two blocks, called Analog Chip Bottom (ACB) and Digital Chip Bottom (DCB), are integrated underneath the pixel matrix. The first one includes a number of analog IP blocks, mainly conceived for providing the pixel matrix with the proper bias setting. It also integrates blocks for the monitoring of different signals, temperature and radiation sensors, clock/data recovery circuits, the serializer and power on reset blocks. All these circuits have been thoroughly tested, also from the standpoint of radiation tolerance, before their integration into RD53A. An additional task of the ACB is to provide two DC voltage levels for the in-pixel calibration circuit described in section 3.2. On the other hand, the Digital Chip Bottom integrates the blocks that implement all the control and processing functionalities, and it is driven by clock signals generated in custom layout blocks that are part of the ACB.

3. Analog front-ends

Three analog front-end (AFE) flavors are integrated, as already mentioned, in the RD53A chip. These are improved versions of readout chains formerly integrated in small prototype chips, namely CHIPIX65 [3] and FE65-P2 [4]. A summary of the test results relevant to the front-ends integrated in these small-scale prototypes was presented by the authors in [5]. An overview of the RD53A AFEs is provided in the following, along with a description of the main improvements implemented with respect to the channels described in [5], and the first preliminary test results.

3.1. Synchronous, Linear and Differential front-ends

The Synchronous analog front-end is an improved version of the CHIPIX65 synchronous channel [6]. It consists of a single stage charge sensitive amplifier (CSA) with a Krummenacher feedback network providing both the feedback capacitor constant current discharge and the sensor leakage current compensation. The charge preamplifier is AC coupled to a synchronous discriminator including a positive feedback latch. The latch can be turned into a local oscillator running up to 800 MHz in order

to internally generate a clock that can be used for high-speed ToT digitization. In this design an offset compensation using internal capacitors has been chosen, making it possible to perform a local threshold trimming without the need of a correction DAC. The total current consumption of the front-end, including the latch, is close to 5.5 μA.

The Linear front-end is an improved version of the CHIPIX65 asynchronous channel [7]. The readout chain includes a charge sensitive amplifier featuring a Krummenacher feedback complying with the expected large radiation induced increase in the detector leakage current. The signal from the CSA is fed to a high-speed, low power current comparator that, combined with the time-over-threshold counter, is exploited for time-to-digital conversion. Channel to channel dispersion of the threshold is addressed by means of a local circuit for threshold adjustment, based on a 4-bit binary weighted current DAC. The front-end chain is optimized for a maximum input charge equal to 30000 electrons and features an overall current consumption close to 4 μA.

The Differential analog front-end is a continuous-time analog processing channel which implements an improved version of the analog channel integrated in the FE65-P2 chip [4] . It is based on a 2-stage comparator and a charge sensitive amplifier whose input is used as a reference for the comparator's first stage, referred to as the pre-comparator. The analog to digital conversion is implemented entirely in the digital core, by digitizing the time-over-threshold of the comparator output pulse. The CSA stage features a current mirror constant current feedback and the gain can be adjusted by choosing between different values of feedback capacitance. For leakage currents below 10 nA, the continuous feedback is capable of preventing the input from saturating. On the other hand, for larger currents, a leakage current compensation (LCC) circuit has been envisaged. Local tuning of the threshold is performed by exploiting one 4-bit resistor ladder in each pre-comparator branch. The pre-comparator stage is followed by a classical continuous time comparator stage with output connected to the digital pixel region through logic gates. The pseudo-differential design reduces variation due to mismatch and provides improved rejection of power supply and digital activity noise.

As aforementioned, the three RD53A front-ends implement a number of improvements with respect to the analog channels integrated in the CHIPIX65 and FE65-P2 small-scale chips. The main improvements are listed in the following:

- reduced area of the front-end analog macro, enabling the integration of dense in-pixel digital functionalities;
- isolation strategy: two deep N-wells (one for the analog macro and one for the digital) have been adopted in RD53A. The same approach was used in the FE65-P2 prototype, but not in CHIPIX65, where only the analog front-ends were integrated in deep N-wells;
- improved stability of the CSA stage integrated in the three RD53A front-ends;
- dedicated Krummenacher power supply for the Synchronous and the Linear front-ends, which results in a less sensitive ToT with respect to voltage drops on power supplies;
- increase in size of the offset capacitors of the Synchronous front-end to reduce discharge effects caused by leakage currents;
- reduced temperature sensitivity of the Linear AFE thanks to the integration of a new threshold tuning scheme;
- integration of a set of analog inverters for most of the configuration bits of the front-ends, which results in an improved digital noise immunity;
- usage of a new, common calibration scheme with improved functionalities (described in the following).

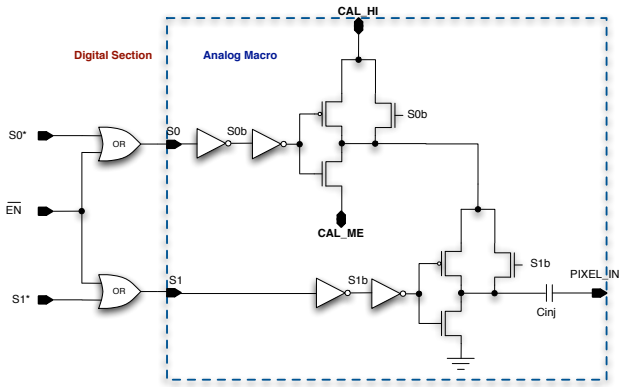

Figure 2: In-pixel charge injection circuit.

3.2. *Injection circuit*

Each pixel of the RD53A matrix integrates the injection circuit shown in Fig. 2. This architecture is common for all the RD53A analog front-ends. The circuit is based on the in-pixel generation of the analog test pulse starting from two defined DC voltages (CAL_HI and CAL_ME), distributed across the matrix and generated with dedicated DACs in the ACB, and a third level, corresponding to a local analog ground. Two operation modes are envisaged for the injection circuit, which make it possible to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time.

The injection circuit enables the fundamental analog tests of the RD53A chip that are being carried out by means of purposely developed testing systems, called BDAQ53 and YARR. Presently, both the analog and digital operation of the chip is being investigated and many test routines have been developed for this purpose.

4. First test results

Fig. 3 shows the S-curves for the sub-matrix featuring the Linear front-end flavor as obtained after tuning carried out at a threshold close to 1000 electrons. Similar results have been obtained for the Synchronous and the Differential front-ends. The

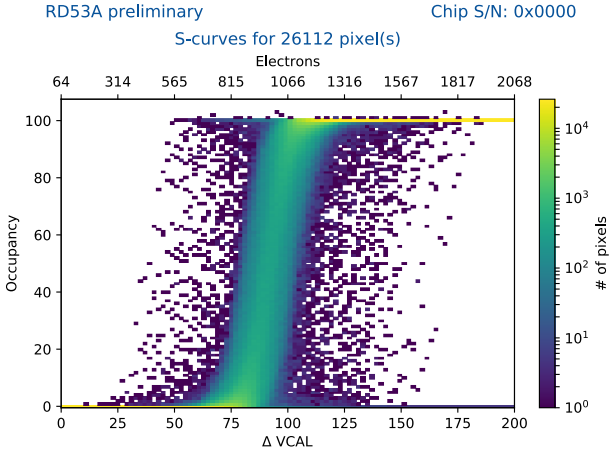

Figure 3: S-curves for all linear front-end pixels after tuning at threshold around 1000 electrons.

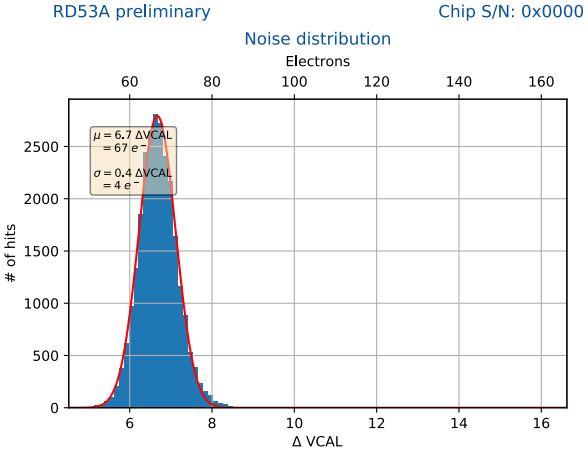

Figure 5: Noise distribution of the Linear front-end pixels.

main analog performance parameters can be directly derived from S-curves data fitting. In the threshold distribution plot, shown in Fig. 4, the threshold values obtained from the S-curve fits are histogrammed and a Gaussian distribution is fit to the data to obtain the mean threshold and the threshold dispersion for the pixels featuring the Linear front-end flavor. In this example, the mean threshold is slightly smaller than 1000 electrons, with a threshold dispersion around 50 electrons. Noise performance is here evaluated in terms of the equivalent noise charge (ENC), whose distribution is shown in Fig. 5, again, for the Linear AFE channels. A mean value of 67 electrons has been obtained in this test. The three front-end architectures are fully functional and feature moderately different performance from the standpoint of noise, minimum threshold, threshold dispersion and charge-ToT conversion. Nonetheless, they can be operated at stable thresholds significantly smaller than 1000 electrons, with ENC and threshold dispersion not exceeding 100 electrons for the non-irradiated, bare chips. A comprehensive characterization of the chip is on-going, including tests after irradiation at total ionizing dose levels up to 500 Mrad(SiO_2).

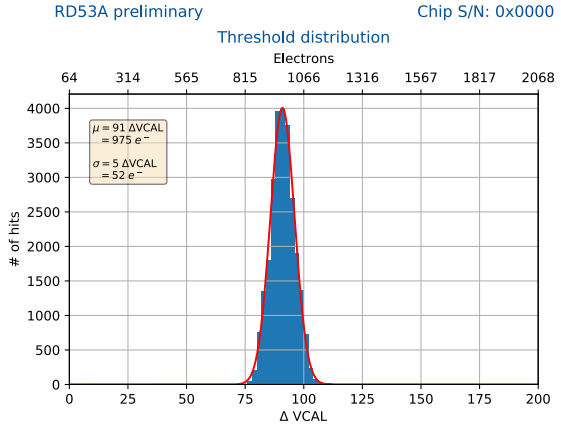

Figure 4: Threshold distribution of the Linear front-end pixels after tuning performed at 1000 electrons.

5. Conclusions

The RD53A demonstrator has been submitted in August 2017 in the framework of the RD53 Collaboration in a 65 nm CMOS technology. The RD53A chip, including a 400 × 192 pixel matrix, is being thoroughly characterized and preliminary test results are very promising. The RD53B design framework, involving around 20 designers, has been established in view of the development of the final pixel chips for ATLAS and CMS with a submission planned for 2019.

6. Acknowledgement

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References

[1] RD53 web site, http://rd53.web.cern.ch/rd53/
[2] L. J. Casas et al., "Characterization of radiation effects in 65 nm digital circuits with the DRAD digital radiation test chip", Journal of Instrumentation, vol. 12, no. 02, p. C02039, 2017.
[3] N. Demaria et al., "CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments", *Proceedings of the 2015 6th IEEE International Workshop on Advances in Sensors and Interfaces, IWASI 2015*, pp. 49-54, Aug. 2015.
[4] M. Garcia-Sciveres et al., "Results of FE65-P2 Pixel Readout Test Chip for High Luminosity LHC Upgrades", PoS ICHEP2016 272 (2016)
[5] L. Gaioni et al., "Design of analog front-end for the RD53 demonstrator chip", Proceedings of Science, PoS (VERTEX2016) 036.
[6] E. Monteil et al., "A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC", *Journal of Instrumentation*, vol. 12 C03066, Mar. 2017, doi: 10.1088/1748-0221/12/03/C03066.
[7] L. Gaioni et al., "65 nm CMOS analog front-end for pixel detectors at the HL-LHC", *Journal of Instrumentation*, vol. 11 C02049, Feb. 2016, doi:10.1088/1748-0221/11/02/C02049.