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PROGRAMMED QUADRUPOLE POWER SUPPLIES FOR NINA

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SUMMARY

Power supplies are described which are used to energize quadrupole magnets in an electron synchrotron so that the focus of the beam can be accurately controlled throughout acceleration and extraction.

INTRODUCTION

Four pairs of quadrupole magnets were installed in the 5 GeV electron synchrotron NINA at the end of 1974[1] to allow the beam focusing (betatron Q-values) to be controlled precisely throughout the 10 ms of acceleration and extraction. The two magnet current waveforms needed to produce the required Q shifts are calculated by a computer program from known machine parameters and, from a knowledge of the magnet inductance, the voltage waveform is derived. Each waveform is stored as 500 nine bit numbers in a minicomputer which then reproduces the waveforms at a frequency of 53 Hz through a digital-to-analogue converter. The eight power supplies receive these waveforms with a maximum amplitude of 7.5 V and amplify them to 300 V with low output impedance for application to the magnets. The shape and amplitude of the voltage waveforms required varies considerably depending on the degree of Q shift required and the power supplies must be capable of generating all likely waveforms.

Each power supply contains an energy storage inductor from which energy is transferred during the synchrotron acceleration period to a capacitor and hence to the magnet under the control of banks of switching transistors. During the remainder of the cycle most of the energy is returned to the inductor by a similar process. At the beginning of each cycle the relatively small amount of energy lost is replaced from an auxiliary power supply.

Control of the circuit is achieved by comparing the voltage developed across an auxiliary winding on the magnet with the incoming reference waveform. If the error exceeds 1% of the peak amplitude the transistors are switched in such a way as to reduce the error. When the error is reduced to zero the circuit is allowed to idle until the error builds up to 1% again. It follows that the voltage waveform contains a 1% saw-tooth superimposed on the required waveform but the magnet current waveform is smoothed by the action of the magnet inductance.

CIRCUIT DESCRIPTION

A simplified schematic diagram of the power supply for one quadrupole magnet is shown in fig.1 and its operation is as follows. Assume initially that a steady current is circulating through T2, D1 and the energy storage inductor and that the magnet current and capacitor voltage are zero. Assume also that T1, T3 and T4 are non-conducting. If T2 is now switched off the inductor current will be diverted through D2 and the capacitor C causing the capacitor voltage to increase at a rate determined by the inductor current and the capacitance of C. When T2 is

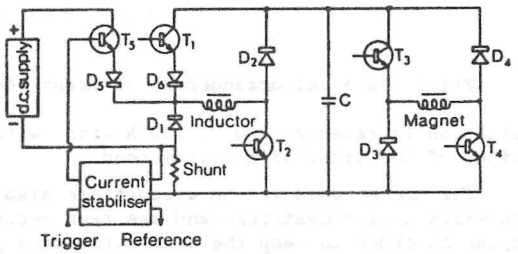

Fig.1 Simplified schematic diagram of power supply.

switched on again the current will circulate through T2, D1 and the inductor and the capacitor voltage will remain constant. By switching T2 on and off at the correct instants the mean rate of increase of capacitor voltage can be controlled. In a similar way the mean rate of decrease of capacitor voltage can be controlled by switching T1 on and off at the correct instants while T2 is in a conducting state. Thus, within certain limits, any positive capacitor voltage waveform can be obtained by suitable switching of T1 and T2.

This voltage waveform is applied to the magnet at injection by switching on transistors T3 and T4. The magnet current will then be proportional to the integral of the voltage. It is possible to produce only positive voltages across the capacitor, however, if current is already flowing in the magnet, the magnet voltage can be reversed by merely switching off transistors T3 and T4 to allow the current to flow through D3, D4 and the capacitor. The magnet voltage can therefore be of either polarity but the current can only be undirectional.

Transistor T5 is connected to the auxiliary power supply and is switched on for a short period at the beginning of each cycle to restore the current to a predetermined level. Two additional diodes are required in series with transistors T1 and T5 to prevent the flow of reverse current in these transistors.

Each transistor shown in fig.1 is in fact a bank of 15 transistors arranged as shown in fig.2 and mounted on a water cooled heatsink. One transistor in each bank is used as a driver for the remaining 14 transistors which have emitter resistors to help share the current more equally between them. The base-emitter voltage of the main transistors plus the emitter resistor volt-drop provide a negative bias for the drive transistor during switch-off and this helps to keep the storage time of the drive transistor short. The storage time of the main transistors is low because overdrive of their bases is prevented by the reduction in gain of the drive transistor as the collector voltage falls. The com-

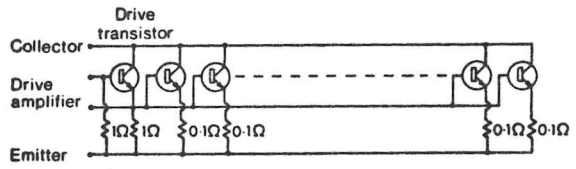

Fig.2 Parallel arrangement of transistors.

bination is rated at 300 V, 100 A with switching times of the order of a microsecond.

The diodes used in the circuit are also mounted on water-cooled heatsinks and are fast-recovery types in order to keep the transistor dissipation low.

The rate of change of current in the transistor is very high and any excessive stray inductance in the circuit will give rise to high voltage spikes which could damage the semiconductors. To prevent this the interconnections are made of Mylar covered copper straps and the go and return leads to each transistor and diode are run as close together as possible.

DRIVE AMPLIFIERS

The drive amplifiers convert the normal TTL level signals from the control circuitry to a level suitable for driving the transistor banks and also provide the isolation required for driving transistor banks T1, T3 and T5 which have un-earthed emitters. The outputs of the drive amplifiers must have fast rise and fall times to keep the switching losses in the transistor banks to a minimum. Since the input resistance of the transistor banks is low care must be taken to ensure that the inductance of the connections between the drive amplifiers and the transistor banks is sufficiently low. Each drive amplifier is therefore mounted as close to its transistor bank as possible and the connections are made of parallel strips of Mylar insulated copper.

The circuit of a drive amplifier is shown in fig.3. Storage time effects in the power transistors

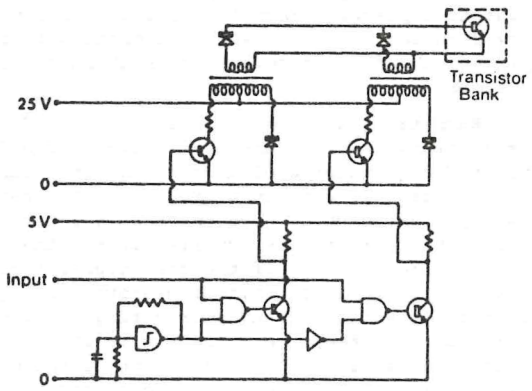

Fig.3 Schematic diagram of drive amplifier.

provide overlap between the pulses so that there are no communication notches in the output.

WAVEFORM STABILIZER

A simplified schematic diagram of the waveform stabilizer is shown in fig.4. The reference waveform from the waveform generator passes through a unity gain inverting buffer amplifier before being compared with the waveform fed back from an auxiliary winding on the quadrupole magnet. The difference between the two waveforms is amplified by an error amplifier with a gain of three and appears at the inputs of two Schmitt trigger circuits.

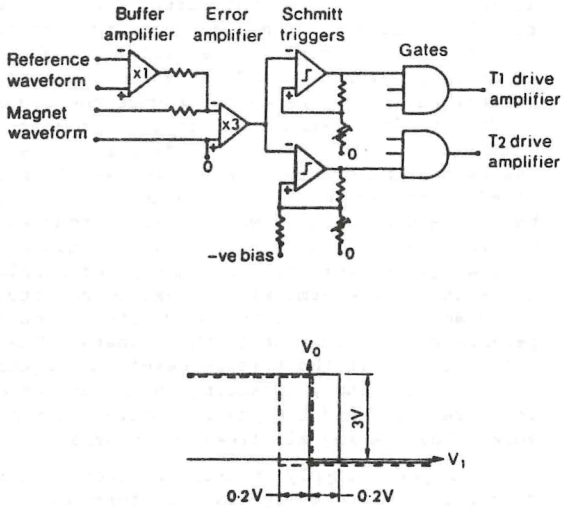

Fig.4 Simplified schematic diagram of waveform stabilizer.

The amplifiers in these two circuits are level detectors whose outputs change rapidly between two saturated levels of approximately 0 V and 3 V as their inputs pass through zero. The characteristics of the complete Schmitt circuits are shown in fig.4. Consider first the full line characteristic which refers to the upper Schmitt circuit in the figure. When the input voltage V_1 is negative the output voltage V_0 is positive and a fraction of this output voltage is fed back to the non-inverting input of the amplifier by the potential divider. If the input voltage is gradually made more positive the output will remain positive until the voltage at the inverting input is equal to the voltage at the non-inverting input when the output will switch to zero. Further positive excursions of the input voltage cause no change in the output. The voltage at the non-inverting input is now zero and the input must be reduced to this level before the circuit switches back to its original state. The horizontal width of the characteristic is adjusted by means of the variable resistor to be 0.2 V. The dotted characteristic refers to the lower Schmitt circuit in the figure and is biased so as to move the whole characteristic to the left by 0.2 V. The outputs of both circuits pass through gating circuits, shown greatly simplified in the figure, to T1 and T2 drive amplifiers.

If the voltage feedback from the magnet is too low the output of the error amplifier will be above 0.2 V and the outputs of both Schmitt circuits will be low causing T1 and T2 to be switched off. This is the condition which will cause the magnet voltage to increase. As the voltage fed back increases, the output of the error amplifier will decrease until it reaches zero, when the upper Schmitt circuit output will become positive and T2 will be turned on thus preventing further increase of the magnet voltage. In a similar way, if the output of the error amplifier becomes more negative than - 0.2 V indicating that the magnet voltage is too high, the outputs of both Schmitt circuits will be high, T1 and T2 will conduct and the magnet voltage will be reduced.

The gate circuit performs a number of functions. It allows the waveform stabilizer to operate during the 10 ms of acceleration and in conjunction with a combination of timing circuits and voltage limiters controls the recovery of energy from the magnet during the remainder of the cycle. It reverses the signals to the transistors if a negative reference voltage is present. It allows the capacitor voltage to be preset before injection by means of an auxiliary stabilization loop. Finally it inhibits T5 from conducting during the switching on process thus limiting the inrush current.

ENERGY RECOVERY

At the end of acceleration and beam extraction, which lasts for up to 10 ms, some or all of the energy has been transferred to the magnet and it must be returned to the energy storage inductor during the remaining 8.9 ms of the cycle. A timer switches the circuit to the recovery mode 10 ms after injection and the following 6 ms is devoted to the first phase of energy recovery during which the magnet current is reduced to zero. The last part of the cycle is devoted to reducing the capacitor voltage to the level required at the start of the next cycle.

To reduce the magnet current to zero as quickly as possible T3 and T4 are switched off so that the current flows through D3 and D4 and as high a voltage as possible is made available across the capacitor. The capacitor voltage increases due to the magnet current flowing through it but the rate of increase could be quite low if the magnet current happened to be low. The rate of rise of capacitor voltage is therefore increased by charging also from the energy storage inductor by switching T1 and T2 off. If this condition were allowed to continue the capacitor would become charged to a voltage in excess of the transistor ratings so a voltage limiting circuit is included. The voltage limiting circuit detects two levels of capacitor voltage, one at 300 V and the other a few volts higher, both circuits having about 1% of backlash. When the lower level is reached T1 and T2 are switched on, returning current to the energy storage inductor. What happens to the capacitor voltage after this depends on the relative magnitudes of the currents in the magnet and inductor. If the magnet current is lower than the inductor current the voltage will fall until the backlash is taken up, and then T1 and T2 will switch off again and the voltage will rise. The capacitor voltage is thus kept within 1% of 300 volts and the magnet current falls linearly to zero, reverse current being prevented by diodes D3 and D4. On the other hand, if the magnet current is greater than the inductor current the capacitor voltage will continue to rise after the first level has been reached. When the second level is reached T4 is switched on, the magnet current circulates through T4 and D3, and, because current is still flowing through the inductor, the voltage falls until the backlash in the upper level detector is taken up. The capacitor voltage is thus kept within 1% of the upper level until the inductor current exceeds the magnet current when the circuit changes to lower level operation as above.

After 6 ms of this phase of recovery T1 and T2 are switched on and because the inductor current is high by this time the capacitor voltage falls rapidly to the required injection level. The magnet current normally reaches zero during the first phase of recovery but it can occur after this time if the peak magnet current is high.

CONCLUSION

A wide range of waveforms can be generated by the power supplies but there are some limitations on the rate of change of voltage which can be achieved. Attempts to exceed these limits will not damage the power supplies but their outputs will be unable to follow the reference waveform. The limits vary throughout the cycle and depend on the shape of the previous part of the waveform. The computer program calculates these limits and if they are exceeded by the demanded waveform prevents the transmission of data to the minicomputer.

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1. N. Marks, J.B. Lyall, M.W. Poole, NINA Programmed Quadrupoles. 1975 Particle Accelerator Conference, Washington, March 1975. To be published in Proc. IEEE (NS).