Single Die Process Using Shadow Masks for a 55µm Fine Pitch Array of 4µm-tall Indium Bumps Across an Entire Chip

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***Abstract*—Large area detectors for X-ray science, high energy physics and other radiation applications are generally assembled from multiple hybridized sensor/read-out chip modules. To minimize the dead area between these modules, the detector pixel arrays on sensor and read-out chips extended to the periphery of each chip. Conventionally sensors and read-out chips such as Application-Specific Integrated Circuits (ASIC) are processed on wafers using photolithography. A lift-off process is used to create arrays of tall indium bumps (~5µm) for interconnects between sensor and ASIC. After the lift-off process, individual chips are commonly diced from these wafers followed by flip-chip bonding of sensors and ASICs. However, wafer-scale processes are often not suitable for small scale production, R&D processes, and specific detector materials such as CdZnTe that is typically provided as individual die. As an alternative to wafer-scale production, small numbers of single dies are processed for interconnect deposition and flip-chip bonding. For dies with large pixel pitch (~250µm), printing arrays of epoxy-based silver (Ag) dots is suitable for forming flip-chip interconnects, but this process has limitations and requires gold (Au) studs on the pairing ASIC array. For smaller pixel pitch, indium bumps are desirable and have also the advantage that a cold-welding at room temperature can be used for flip-chip bonding. Forming indium bumps on single die with lift-off photolithography is not trivial when the array expands to the periphery of the die. Due to surface tension an edge bead of the photoresist (PR) builds up creating a non-uniform PR thickness across the die which impedes the formation of uniform PR openings. Using a shadow mask instead of the PR is a suitable alternative for processing a single die. The mask is mechanically aligned and placed over the die and removed after the indium deposition. Electroformed and etched shadow masks with different thickness and aperture openings were tested for the indium deposition on single chip dies. Ultimately, we demonstrate an array of 4µm-tall indium bumps on a pixel pitch of 55µm. This fine pitch is essential for X-ray radiation detectors, such as Medipix, which utilize ASICs in a 256×256-pixel array for scientific applications. This shadow mask process is not only useful for minimizing the dead area between chip modules in edgeless radiation detectors, but also for other applications where samples do not sustain standard lithography procedures or when processing of single dies is required.**

Keywords—indium bump deposition, single die, shadow mask, lift-off lithography, flip-chip bonding, MEDIPIX

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I. Introduction

Flip-chip bonding and indium bump bonding among other bond processes for microelectronic packaging are essential techniques of the heterogeneous integration and hybridization of pixel sensors and read-out ASICs of radiation detectors such as HEXITEC, LPD, and Medipix [1,2,3]. Pixel arrays of such sensors and ASICs reach to the periphery of each chip so that the dead area between butted chips for large area detectors is minimized. Indium is a pliable material suitable for interconnects that allow cold-welding of pixel arrays of sensors and ASICs in a flip-chip process. In order to form indium bumps, a photolithographic lift-off process is usually carried out on wafers that comprise multiple sensor and ASIC chips. After indium deposition and stripping of the lift-off PR, tall (~5µm) indium bumps remain on the desired pixel arrays. Chips are singulated from the wafer and subsequently flip-chip bonded in order to create hybrid sensor/ASIC modules that are further assembled (e.g. wire bonding to a PCB) and integrated in the detector system. Details of such hybridization process with indium bumps are described in [4].

The conventional wafer-scale epitaxial lift-off process may not always be suitable or applicable for assembly processes that involve individual single dies, especially in scenarios such as small-scale production, research and development (R&D), and specific detector materials (e.g. CdZnTe). Stencil printing of electrically conductive epoxy filled with high content (≥ 90%) of Ag particles directly onto the pixel array of a die is an adequate alternative process for single dies with large pixels and pitch-size (≥ 250µm) [5]. However, this process requires studded pixel arrays on the pairing chip for sufficient electrical conductivity and spacing between hybridized sensor/ASIC chips [5]. Despite significant efforts in technology development [6], commercially available conventional manufactured stencils and conductive epoxies do not achieve sub-100µm pixel and pitch sizes consistently. However, such stencils can be used as shadow masks for indium bump deposition.

Spin-coating photoresist (PR), which is commonly used in photolithography, onto a single die is not straightforward when aiming for uniform PR layers. The challenge arises from the formation of a bead at the edges of the die during the spin-coating process. In wafer processing this PR edge bead is commonly removed at the wafer periphery which does not

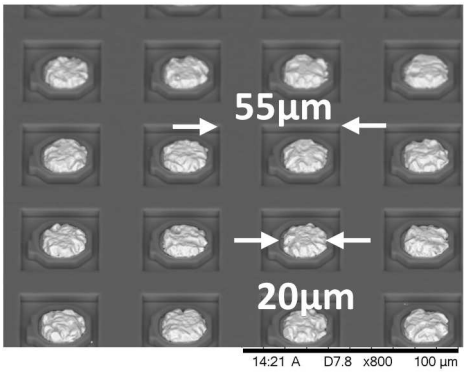

Fig. 1. SEM image of a typical indium bump array on 55µm-pixel-pitch fabricated with photolithography after lift-off of PR.

include any chip pattern. This edge bead removal method is unusable for single dies where the pixel pattern extends to the die's periphery in an attempt to minimize any dead areas. Therefore, it is desirable to substitute the PR with a rigid shadow mask for single die processing. This paper investigates different masking techniques for indium deposition, including photolithography with photoresist (PR), electroformed masks, and etched Si membranes with apertures.

II. Methods for Indium Deposition

A. Lift-off Photolithography

One of the common processes for depositing pattern like conductor lines, pixel bumps, or any form of structured metallization on semiconductors for electronic circuitry is to perform lift-off photolithography on wafers. A general description of the process can be found in [7] and in particular for the deposition of indium bumps in [4]. Equipment for wafer priming (YES HMDS oven), PR spin-coating (SUSS Gyroset) and PR exposure (SUSS MA8 mask aligner) including hot plates and wet-chemical development utensils are used in a clean room of the Innovations - Technology Access Centre (ITAC) at STFC-RAL. Typical indium bumps (20µm-diameter, ~5µm height) which were deposited on a 55µm-pitch pixel array using wafer-scale lift-off process are shown in Fig.1.

B. General Shadow Mask Technique

Using shadow masks for patterning any kind of substrate is well-known and applied in various different fields of technology. Early description of this method for patterning semiconductors with thin metal structures was reported in [8]. Here we use the method to deposit tall bumps (~4µm) of indium as interconnect material on single die for subsequent thermal-compression flip-chip bonding. The apertures of such shadow masks are optically aligned to the pixel array of sensor or ASIC chip which are mounted in a custom-made jig that can hold chip and shadow mask. After alignment, the mask is temporarily fixed to jig and chip. The whole jig assembly with chip is transferred to a thermal evaporator (MPS800 indium evaporator) for the indium deposition. Several of such jigs that contain each a masked chip can be deposited with indium simultaneously. The evaporator system is enabled for an in situ argon plasma cleaning process and deposition of a 10nm-thin Cr adhesion layer prior to the indium deposition.

C. Electroformed Shadow Masks

For sensor/ASIC dies with arrays of pixel-pitch greater than 100µm, STFC-RAL currently utilizes electroformed shadow masks. These masks are produced by ASMPT-DEK and manufactured like nickel electroformed stencils for stencil printing processes as described in the paper's introduction. These shadow masks are designed and machined in such a way that they fit together with the sensor/ASIC chip in a customized jig that can be loaded into the indium evaporator. According to ASMPT-DEK [9], electroformed shadow mask stencils are limited in pitch and aperture size due to their fabrication method. The smallest aperture dimensions that the current manufacture provides are restricted to electroformed masks with apertures of (50±4)µm openings and a minimum distance of 50µm between apertures [9]. The typical thickness of such mask is approx. 50µm.

D. Si-etched Shadow Masks

Due to the limited aperture and pitch size of the electroformed masks, Kelvin Nanotechnology Ltd. fabricated Si membranes with precision-etched apertures to demonstrate the deposition of indium bumps with smaller pitch on a single die. Initially several 4-inch ~380µm-thick Si wafers with 9 different arrays of 256×257 apertures (55µm-pitch) on thin membranes were produced. At first, 100µm- and 50µm-thin membranes of approx. the size of 15mm×15mm were wet-chemically etched into the Si wafers. Subsequently photolithography and Deep Reactive Ion Etching (DRIE) was used to fabricate apertures in those membranes. In order to investigate the deposition process with these Si membranes, different diameters of apertures were chosen (45µm to 25µm). For simplicity, single dies were initially temporarily bonded to larger carrier chips. Then, during Si mask and chip alignment, these carrier chips were directly glued to the Si

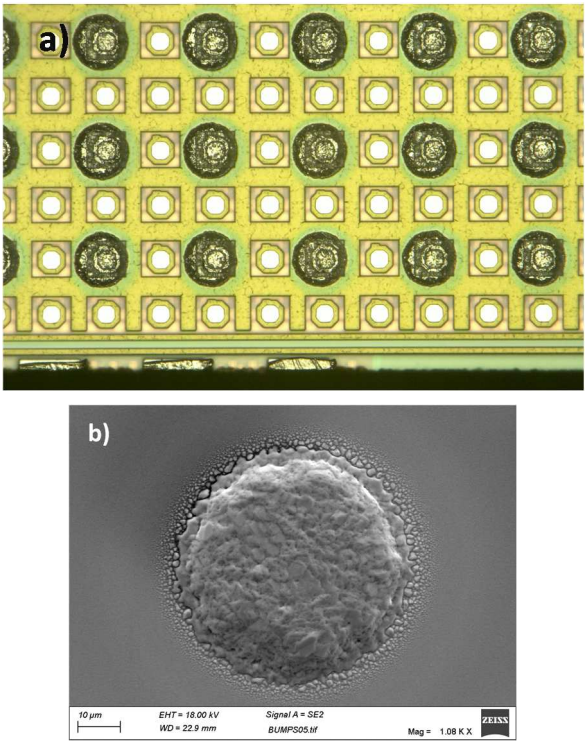

Fig. 2. a) Photo of a 55µm-pitch ASIC-pixel array with indium bumps on 110µm-pitch at the ASIC edge (indium deposited with electroformed shadow mask). b) SEM image of a similar indium bump also deposited using an electroformed shadow mask.

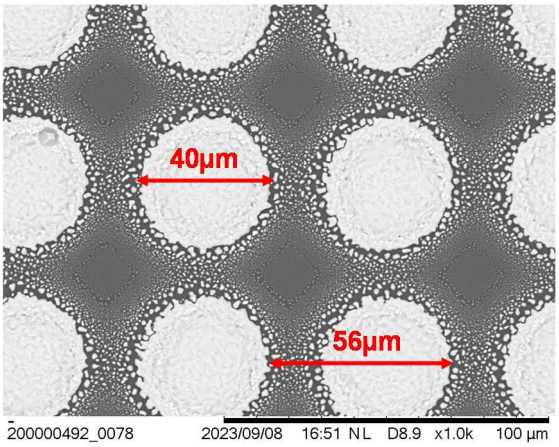

Fig. 3. Indium bumps deposited through a Si shadow mask with 100µm-thick membrane and 35µm-diameter of apertures.

wafer aligned to the apertures of the membranes. The wafer with the attached chip and carrier was mounted into the indium evaporator. After deposition, the indium-decorated chip is released from wafer and carrier chip using acetone. Details about these test Si membrane shadow masks and the temporary die attachment were reported in [10].

III. Deposition Results

A. Deposition with Photolithograpy

In recent years, the indium deposition with photolithography is routinely used by STFC-RAL for fine-pitch arrays of sensors and ASICs on wafers up to 8-inch as demonstrated in Fig.1. Subsequently singulated ASICs and sensors with dimensions of up to 50mm×50mm can be hybridized using the SET FC150 or FC300 flip-chip bonder. Alternatively, multiple chips (max. 50mm×50mm) can be flip-chip bonded onto substrates, such as wafers up to 8 inches (200mm × 200mm) using the FC300. The option and ability to use formic acid for an in-situ reflow process is currently being investigated at STFC-RAL with the FC300.

B. Deposition with Electroformed Shadow Masks

The deposition with electroformed shadow masks produces comparable results to the deposition using photolithography if the bump size is about 50µm in diameter and the pitch is greater than 100µm. Therefore, using such masks is a viable method to deposit indium bumps on single die without photolithography. A typical example of such indium bumps on pixels of an ASIC (pixel pitch 55µm) are shown in Fig. 2a. The indium bumps are on a 110µm-pitch and the bump diameter is slightly larger than the ASIC pixel opening. It was not possible to deposit indium bumps on each ASIC pixel due to the limitations of electroformed shadow masks. A magnified view of such pixel is shown in the SEM image (Fig. 2b). Here a shallow ring of indium around the main bump is visible. This ring is possibly formed because the mask is only in close proximity to the chip and indium is scattered at the edge of the aperture edge of the mask during deposition. We reported similar observations in [10].

C. Deposition with Si-etched Shadow Mask

For the deposition of small indium bumps on single die with 55µm-fine-pitch which is a typical application of Medipix X-ray detectors [3], we chose Si-etched membrane shadow masks as described in section II.-D of this paper. In order to initially identify the most suitable aperture size and membrane thickness of such masks for the deposition, a blank 4-inch wafer was clamped behind a Si test shadow mask that included a variety of aperture sizes. Indium deposition onto the blank wafer was performed through the mask's apertures using wafers with varying membrane thicknesses (50 µm and 100 µm). No substantial difference in indium bump sizes and indium that surrounds each bump was found for different membrane thicknesses. However, significant differences in relation to the aperture diameter were detected. The shallow indium halo ring around each main indium bump which was already observed with electroformed shadow masks, has considerably increased in size. For all mask apertures apart from the smallest 25µm aperture diameter, the scattered indium around the main indium bumps is so dense that potentially electrical shorts to adjacent bumps across the whole array were created (Fig.3). The deposition through 25µm-aperture again shows some scattered indium around the bumps but no connection between bumps is visible (Fig.4). The membrane of the array with 25µm-apertures was not in the centre of the initial Si test wafer. Therefore, it is likely that a larger proximity gap between mask and blank wafer at the wafer edge as well as the less collimated off-centre indium deposition caused this remaining scattered indium around the bumps. Hence the deposition experiment through a new shadow mask wafer with a 100µm-thick membrane and 25µm-apertures in the centre of the wafer was repeated on a single die. The single die was attached to the shadow mask

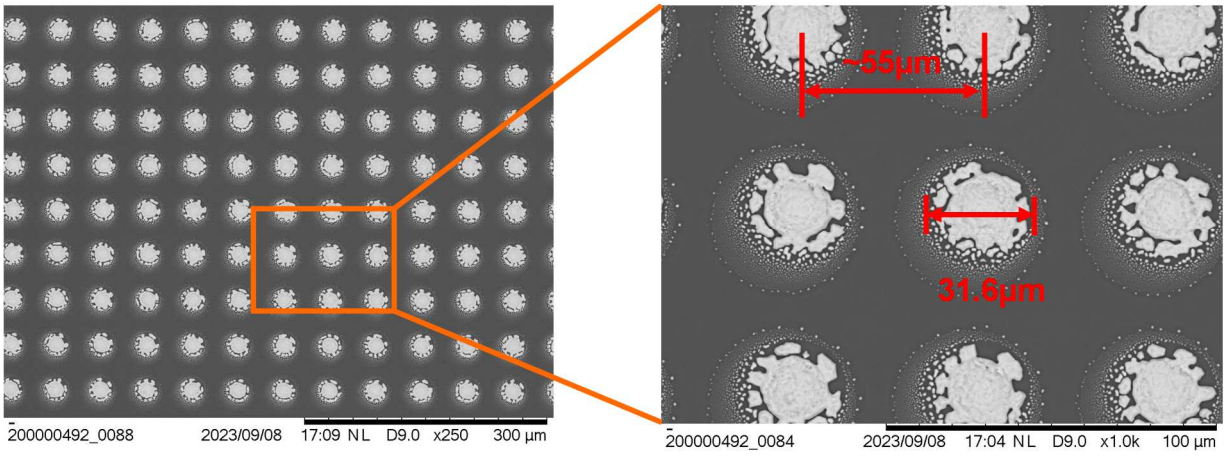

Fig. 4. SEM images of an array of indium bumps deposited on a blank wafer through a Si shadow mask with 100µm-thick membrane and 25µm-diameter of apertures.

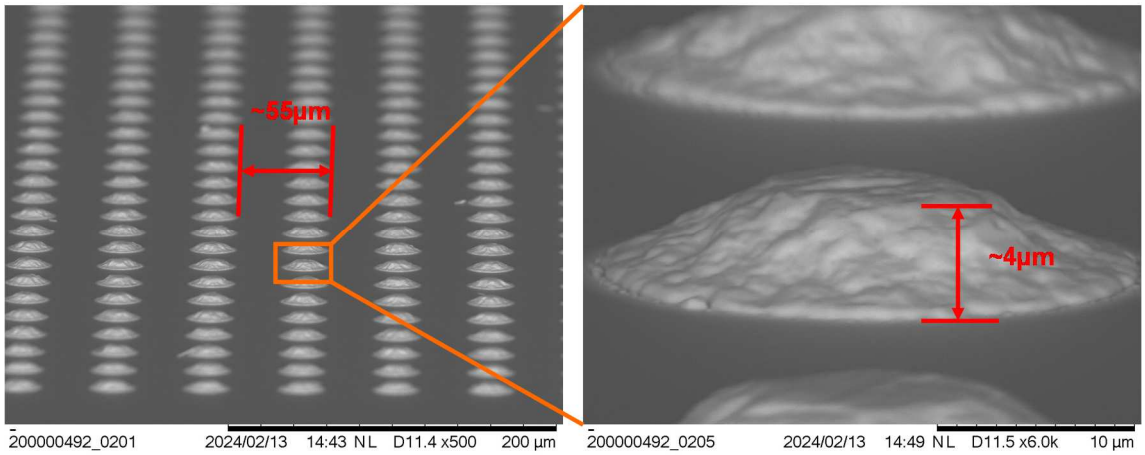

Fig. 5. SEM images of an array of indium bumps on a single die through a Si shadow mask with 100µm-thick membrane and 25µm-diameter of apertures.

wafer as described in II.-D. The results are shown in Fig.5 and indicate much improved indium bump shapes with insignificant scattered indium on such single die. Currently we are assessing if a dilute acid solution will remove the indium from the Si shadow masks so that these masks can be reused.

D. Radiation measurements of hybrid detectors

So far, only a few sensors and ASICs which were deposited with indium bumps using electroformed shadow masks were flip-chip bonded and further assembled to X-ray detectors. Exposure tests with flat field X-ray radiation of an Am-241 sealed source reveal a uniform signal in all pixels across the array. Details of the radiation results are presented in [11] and indicate a bond yield better than 99.9%.

IV. Summary and Conclusion

This paper presents three different masking methods (photolithographic lift-off, electroformed and etched Si-membrane shadow masks) for the deposition of indium bump arrays across an entire chip, extending up to the chip's edge to minimize dead area. The lift-off technique is suitable for wafer-scale processes of multiple chips that are singulated from the wafer after the indium deposition process. A uniform deposition of an indium array across an entire small single chip die is challenging for a lift-off process due to formation of PR edge beads at the periphery of the chip. Shadow masks are better suited for the uniform deposition of such arrays up to the edges of a single die. Apertures of such masks are optically aligned to the pixel array of the die and clamped in a custom-made jig for the indium deposition. It was demonstrated that commercially available electroformed shadow masks are appropriate for creating indium bump arrays with pixel-pitch greater than 100µm. For applications with sub-100µm-pitch, Si membranes were etched with apertures and used as shadow masks. As a proof-of-concept, single dies were temporarily glued to the wafer of the Si membrane masks for the indium deposition. Arrays of ~4µm-tall indium bumps on a 55µm-pitch on single dies were demonstrated.

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References

[1] M.C. Veale, P. Seller, M. Wilson, E. Liotti, "HEXITEC: A High-Energy X-ray Spectroscopic Imaging Detector for Synchrotron Applications," Synchrotron Radiation News, vol. 31, No. 6, pp. 28-32, November 2018.

[2] A. Koch, M. Hart, T. Nicholls, C. Angelsen, J. Coughlan, M. French, et al.,"Performance of an LPD prototype detector at MHz frame rates under Synchrotron and FEL radiation," J. Inst., vol. 8, p. C11001, Nov. 2013.

[3] R. Ballabriga, M. Campbell, E. Heijne, X. Llopart, L. Tlustos, W. Wong, "Medipix3: A 64 k pixel detector readout chip working in single photon counting mode with improved spectrometric performance," Nucl. Inst. Meth. Phys. Res., vol. A 633, pp. S15–S18, June 2010.

[4] Ch. Broennimann, F. Glaus, J. Gobrecht, S. Heising, M. Horisberger, R. Horisberger, et al., "Development of an Indium bump bond process for silicon pixel detectors at PSI," Nucl. Inst. Meth. Phys. Res., vol. A 565, pp. 303–308, May 2006.

[5] A. Schneider, M.C. Veale, D.D. Duarte, S.J. Bell, M.D. Wilson, "Interconnect and bonding techniques for pixelated X-ray and gamma-ray detectors," J. Inst., vol. 10, C02010, Feb. 2015.

[6] R. W. Kay, S. Stoyanov, G. P. Glinski, C. Bailey, M. P. Y. Desmulliez, "Ultra-fine pitch stencil printing for a low cost and low temperature flip-chip assembly process," IEEE Trans. Components and Packaging Tech., vol. 30, p. 129-136, March 2007.

[7] C. Koch, T. J. Rinke, Photolithography – basics of microstructuring, 2nd ed. Siegl Druck & Medien GmbH & Co. KG, Friedrichshafen, 2020, pp. 64, pp. 123, & pp. 156.

[8] W. Decker, R. Belan, V. D. Heydemann, S. Armstrong, T. Fisher, "Novel low pressure sputtering source and improved vacuum deposition of small patterned features using precision shadow masks," Society of Vacuum Coaters 59th Annual Technical Conference, Indianapolis, IN, U.S.A., p. 95-100, May 2016.

[9] ASMPT Datasheet of "DEK electroform mini LED stencils" in www.smt.asmpt.com/en/products/process-support-products/stencil-technologies/ .

[10] A. Schneider, N. Ghorbanian, D. Burt, J. Hollingham, P. Booker, T. G. Brooks, et al., "Deposition of fine-pitch indium bumps on single die," 24th European Microelectronics and Packaging Conference & Exhibition (EMPC), Cambridge, UK, pp. 1-5, Sept. 2023 doi: 10.23919/EMPC55870.2023.10418408.

[11] A. Schneider, N. Ghorbanian, J. Osborn, S.P. Cross, J.D. Lipp, M.J. French, "Bump deposition techniques for hybrid X-ray detectors," J. Inst., vol. 18, C06009, June 2023.