The Ariel payload electrical and electronic architecture: a summary of the current design and implementation status

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The Ariel Payload electrical and electronic architecture: a summary of the current design and implementation status

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ABSTRACT

Ariel [1] [2] is the M4 mission of the ESA's Cosmic Vision Program 2015-2025, whose aim is to characterize by low-resolution transit spectroscopy the atmospheres of over one thousand warm and hot exoplanets orbiting nearby stars. It has been selected by ESA in March 2018 and adopted in November 2020 to be flown, then, in 2029. It is the first survey mission dedicated to measuring the chemical composition and thermal structures of the atmospheres of hundreds of transiting exoplanets, in order to enable planetary science far beyond the boundaries of the Solar System. The Payload (P/L) is based on a cold section (PLM – Payload Module) working at cryogenic temperatures and a warm section, located within the Spacecraft (S/C) Service Vehicle Module (SVM) and hosting five warm units operated at ambient temperature (253-313 K).

The P/L and its electrical, electronic and data handling architecture has been designed and optimized to perform transit spectroscopy from space during primary and secondary planetary eclipses in order to achieve a large set of unbiased observations to shed light and fully understand the nature of exoplanets atmospheres, retrieving information about planets interior and determining the key factors affecting the formation and evolution of planetary systems.

Keywords: Exoplanets, Transit Spectroscopy, Primary and Secondary Eclipses, Atmospheres, Payload Electronics, Spectrometer, Fine Guidance System, Active Cooler

1. INTRODUCTION

Ariel, the Atmospheric Remote-Sensing Infrared Exoplanet Large-survey satellite, is the ESA's Cosmic Vision M4 mission, selected in March 2018 and adopted by the Agency in November 2020 for a launch in mid 2029, whose aim is to characterize by low-resolution transit spectroscopy and spectrophotometry the atmospheres of over one thousand warm and hot exoplanets orbiting nearby stars.

The Ariel Payload, hosting an IR spectrometer (AIRS – Ariel IR Spectrometer) and a Fine Guidance System (FGS) has been designed to perform transit spectroscopy from space during primary and secondary planetary eclipses in order to achieve a large unbiased survey concerning the nature of exoplanets atmospheres and their interiors and to determine the key factors affecting the formation and evolution of planetary systems. To achieve these objectives, an Active Cooler System (ACS) including a Ne Joule-Thomson cooler, is in addition adopted to provide active cooling capability to the AIRS detectors working at cryogenic temperatures, below 42K.

Ariel will observe hundreds of warm and hot transiting gas giants, Neptunes and super-Earths around a wide range of host star types, targeting planets hotter than ~600 K to take advantage of their well-mixed atmospheres. It will exploit primary and secondary transit spectroscopy in the 1.10 to 7.80 μm spectral range and broadband photometry in the optical (0.50 - 0.80 μm) and Near IR (0.80 - 1.10 μm) by a combined use of AIRS and FGS instruments.

FGS contributes, in particular, to the Spacecraft (S/C) Attitude and Orbit Control System (AOCS) operations and it includes three photometric channels (two used for guiding as well as science) between 0.5-1.1 μm plus a low resolution NIR spectrometer for the 1.1-1.95 μm range. Along with FGS, AIRS provides low resolution spectroscopy in two IR channels: Channel 0 (CH0) for the 1.95-3.90 μm band and Channel 1 (CH1) for the 3.90-7.80 μm range.

The operational orbit of the Ariel spacecraft is baselined as a large amplitude halo orbit around the Sun-Earth system 2nd Lagrangian (L2) point. This virtual point in space is located about 1.5 million km from the Earth in the anti-Sun direction, and is confirming the orbit of choice of many current, like JWST, and future (e.g. PLATO) astrophysical missions, because it offers the possibility of long uninterrupted observations in a fairly stable radiative and thermo-mechanical environment.

The spacecraft will be launched by an Ariane 6.2 rocket from Kourou, in the French Guiana. A direct escape injection is planned in the baseline mission profile and the S/C trajectory, with an inclination close to 0 degrees, foresees a single passage through the radiation belts, presently approximated by a 10.5 hours worst-case half orbit with perigee at 300 km and apogee at 64000 km.

The nominal mission duration is 4 years with a minimum extension of an additional 2 years, for a total mission duration of 6 years at least, for which the spacecraft and its on-board electronics shall be carefully designed.

2. ARIEL PAYLOAD DESIGN OVERWIEV

The Ariel Payload is conceived modular by design (refer to Figure 1). The adopted baseline architecture splits the payload into two major sections, the cold payload module (PLM) and the items of the Payload hosted within the spacecraft service module (SVM), i.e. the warm electronics units.

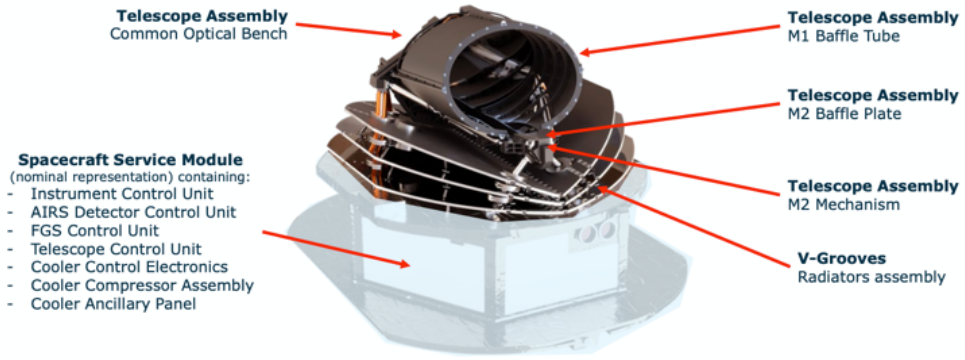

Figure 1: Illustration of the Ariel Payload Module (PLM, top) and Service Module (SVM, bottom) composing the whole Spacecraft (courtesy ADS – AIRBUS Defence and Space).

The PLM is supported by three bipods mounted onto the Payload Interface Panel (PIP). They are hollow cylinders, made of CFRP (Carbon Fiber Reinforced Polymer) filled with low thermally conductive rigid foam. Three Planck-like V-Grooves (VGs) are adopted as high-efficiency passive radiant coolers, providing the first stage of the PLM cooling system [3]. VGs are made by a simple honeycomb structure of Aluminum alloy, thermally connected to the three bipods (to intercept the conducted parasitic heat leaks through the mounting bipods) and are mechanically supported and thermally decoupled from the PIP by GFRP (Glass Fiber Reinforced Polymer) struts.

The telescope, part of the TA (Telescope Assembly) [4], is based on a Cassegrain design with a parabolic primary (M1) and a hyperbolic secondary mirror (M2) plus a third mirror M3 used to re-collimate the beam. A fourth mirror M4 directs the collimated beam onto the optical bench, within the Instrument Cavity (IC) where a common optics and dichroics set is located in order to feed AIRS and FGS optical modules. M2 is supported by a refocusing mechanism with three degrees of freedom (focus and tip/tilt). The purpose is to correct for one-off movements due to launch loads and cool-down and potentially to make occasional adjustments (for example to compensate for any long-term drifts in structural stability). As M2 is moved, also the position of the star (and its spectrum) moves on AIRS and FGS. Because FGS closes the AOCS loop, this ensures that the star is kept onto the slit at all times during any focusing operation.

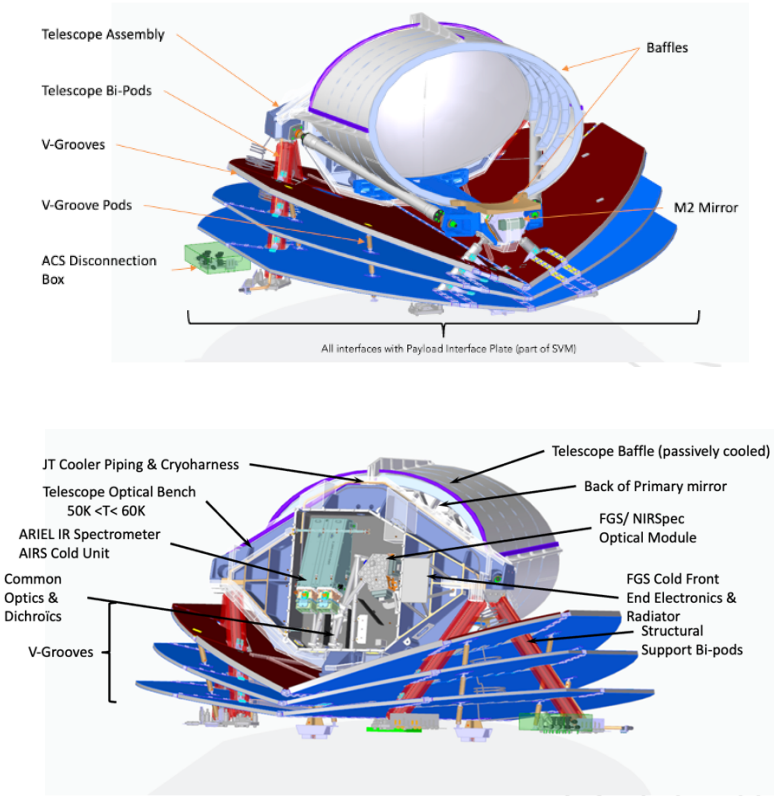

Figure 2: The Ariel cold Payload section (PLM). Top: front view. Bottom: rear view showing the IC content.

With reference to the simplified block diagram of the Ariel Payload Electrical and Data Handling Architecture in Figure 3, the Payload is composed of two instruments, AIRS [5] [6] and FGS [7] [8] plus the Active Cooler System.

AIRS is located at the intermediate focal plane of the Ariel telescope and common optical system and it hosts two HgCdTe-based hybrid IR detectors and two analogic cold front-end electronics (CFEE) for detectors interfacing and readout. Each CFEE is driven by a Detector Control Unit (DCU) part of AIRS but externally interfaced and managed by the Instrument Control Unit (ICU) of the Payload [9] [10] [11]. A Telescope Control Unit (TCU) is foreseen in order to readout the PLM operational thermistors and manage the secondary mirror refocusing mechanism (M2M).

Finally, the Fine Guidance Sensor operations are managed by the FGS Control Unit (FCU), as the CCE (Cryocooler Control Electronics) executes the same task for the Active Cooling System, including a heat exchanger (CHX), an ancillary panel (CAP) and a compressor assembly (CPA).

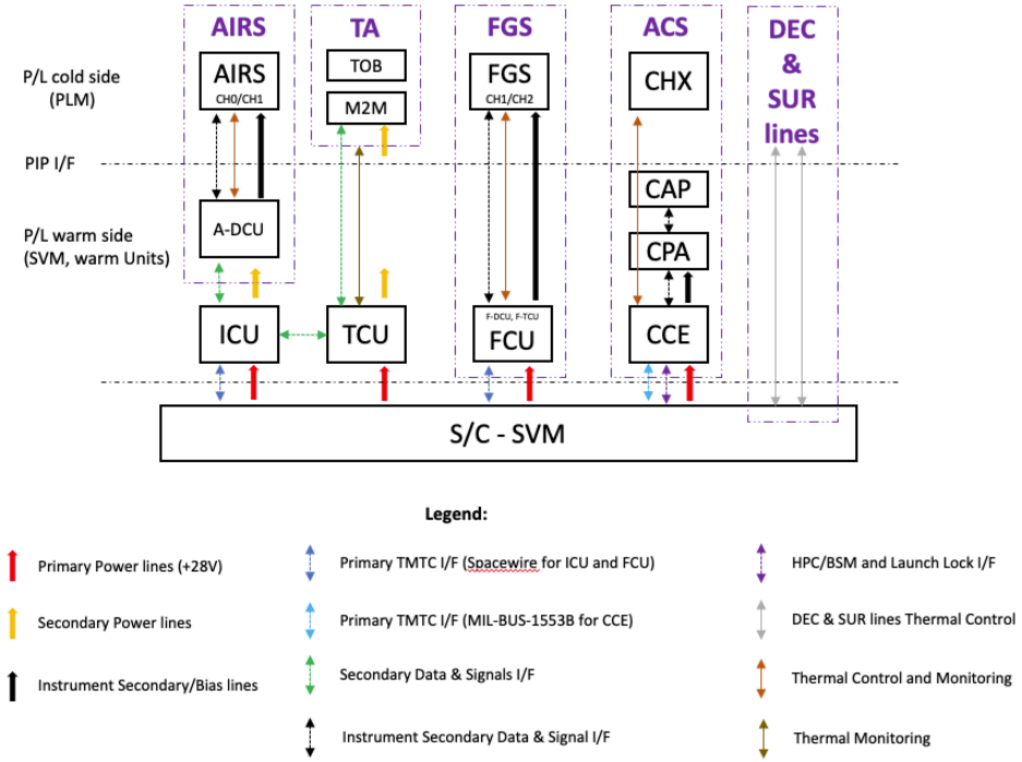

Figure 3: Simplified block diagram of the Ariel Payload data handling architecture

(DEC: decontamination, SUR: survival).

Both ICU and FCU are interfaced with the Spacecraft by means of two Nominal plus two Redundant cross-strapped Spacewire (SpW) I/F running at 10 Mbps plus a N and a R primary power I/F (+28 V). The SpW I/F are used for sending CCSDS PUS telecommands (TC) from the On-board Computer (PBC) and retrieving science and housekeeping telemetries (TM). The ACS is instead managed by means of the MIL-BUS-1553B, 1 Mbps max, interface.

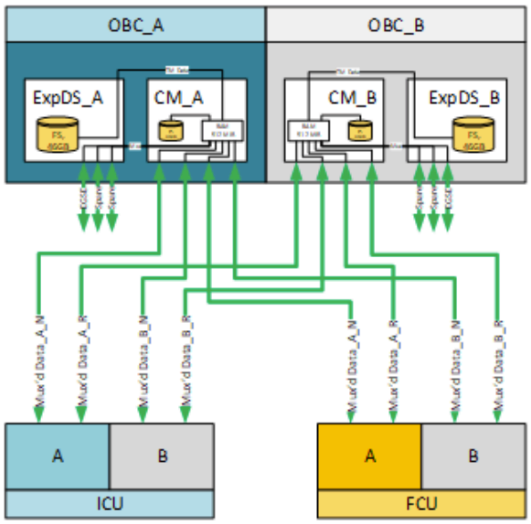

Figure 4: ICU and FCU SpW lines configuration (green lines) to SVM OBC-A (N) and OBC-B (R).

In the following sections, the status of the Payload electrical, electronic and data handling architecture is presented as it is currently conceived following the Payload PDR (pPDR) and in order to face the next P/L milestone: the Critical Design Review (pCDR), expected in Q4 2025.

3. AIRS DESIGN AND IMPLEMENTATION STATUS

AIRS is the Ariel scientific instrument providing low-resolution spectroscopy in two IR channels, CH0 for the [1.95-3.90] µm band and CH1 for the [3.90-7.80] µm band. It is located at the intermediate focal plane of the telescope following the common optical system.
AIRS instrument is composed of three main architectural blocks:

- AIRS Optical Bench (AIRS-OB)
- AIRS integrated Focal Plane Assembly for Channel 0 and Channel 1 (AIRS-iFPA-0 and iAIRS-FPA-1)
- AIRS Detector Control Unit (AIRS-DCU-0 and AIRS-DCU-1)

AIRS-OB and AIRS-iFPA CH0 & CH1 are assembled as a single hardware unit, called AIRS Cold Unit (CU) located in the cold section of the PLM, while the AIRS-DCU-CH0 and AIRS-DCU-CH1 are located in the warm part of the SVM.

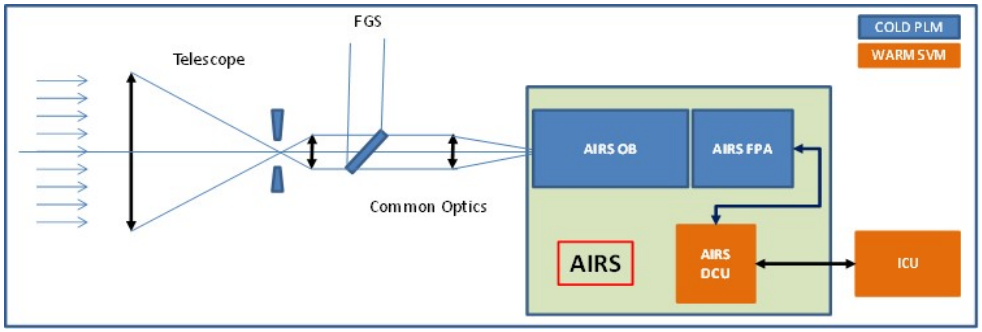

Figure 5: Architectural block diagram of the Ariel Infra-Red Spectrometer.

3.1 AIRS electrical system overview

The electrical system of the AIRS instrument is composed of:

- The two FPAs (CH0 and CH1) including electrical parts for temperature stabilisation of the detectors.
- The two Cold Front-End Electronics (CFEE); one for each detector channel (CH0 and CH1) including electrical parts for temperature stabilisation of CFEE, mounted at the back of each FPA and connected to them by a short low thermal conductivity flex cable. The association of each FPA with its CFEE constitutes an integrated FPA (iFPA).
- The two identical DCU boards; one for each detection channel (CH0 and CH1), assembled in a standalone box mounted in the SVM, called A-DCU. This A-DCU is interfaced with the ICU unit for data and secondary power interface.

AIRS electrical architecture is an assembly of two independent and complete channels, started from the detector and ending with the AIRS-DCU (A-DCU). Only FPA channels differ, in term of spectral range while whole electronics (including the iFPA Cold Front-End Electronics CFEE) and A-DCU for both channels are identical. No redundancy is implemented in the channels to the exception of focal planes thermal control that are duplicated. The AIRS-DCU is then interfacing to the Commanding and Data Processing Unit (CDPU) of the ICU for scientific & housekeeping data

transmission and for the transmission of configuration command. It interfaces with the unit power supply (PSU) that is providing secondary voltage lines. These interfaces with the ICU unit implements cross-strapping to enable coupling of both AIRS channels to redundant functions of this unit. Figure 6 is a representation of this electrical system. Beside interface to the cold AIRS sub-systems, the A-DCU implements inter unit interfaces with the ICU for power supply and control / command functions.

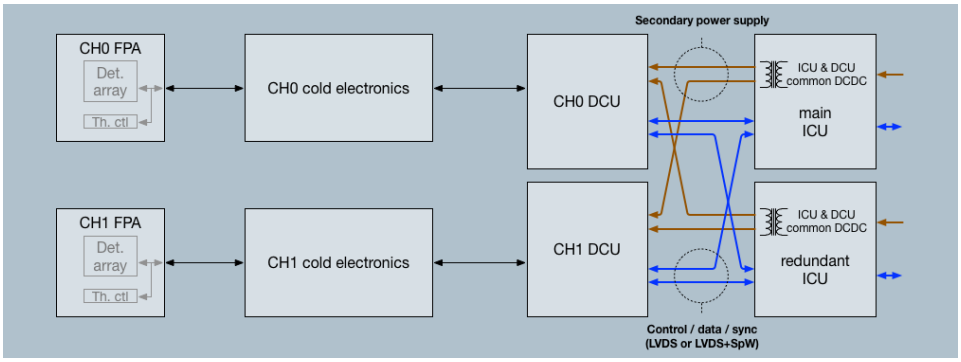

Figure 6: Overview of AIRS electrical system.

The full electronics chain is submitted to various environmental conditions. Detectors are operated at low temperature condition (42 K) thanks to active cryo-cooling. The CFEE units are compatible with a 55 K operating temperature. The A-DCU is operated at ambient temperature condition (operating temperature between 253 K and 313 K with a stability +/-3 K over 10 hours) on the SVM. Additionally, dedicated cryo and warm harnesses sections make the links between the cold sub-systems and between the CFEE and the A-DCU.

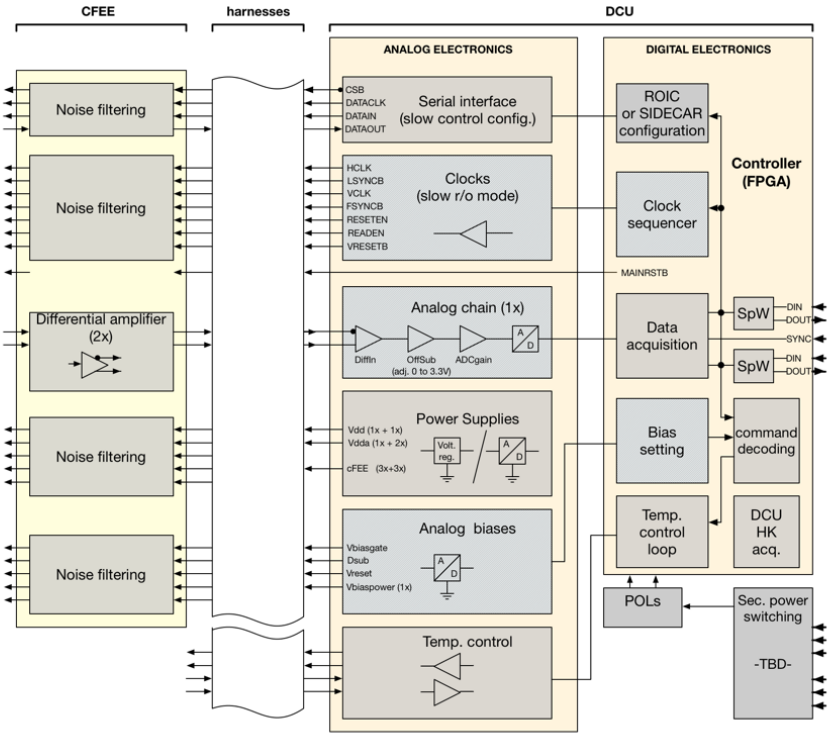

Figure 7: AIRS Electrical Functions Block Diagram.

3.2 AIRS Detectors and cold front-end electronics

The spectrometer is designed to provide Nyquist-sampled spectra in both spatial and dispersion directions to limit the sensitivity of measurements to the jitter noise and intra pixels pattern during the long (order of 10 hours) transit spectroscopy exposures. The thermo-mechanical design of the AIRS instrument has been conceived to work in a 60 K cold environment, with the detection and acquisition chain of both channels based on two HgCdTe detectors actively cooled down below 42 K. CFEE main functionalities are shown in the block diagram reported in Figure 7.

3.3 AIRS Detector Control Unit (A-DCU)

Electrical design of the A-DCU encompasses several high-level functional blocks either analogue or digital. Figure 7 and Figure 8 shown a detailed representation of the block diagram of the unit along with corresponding functions of the CFEE.

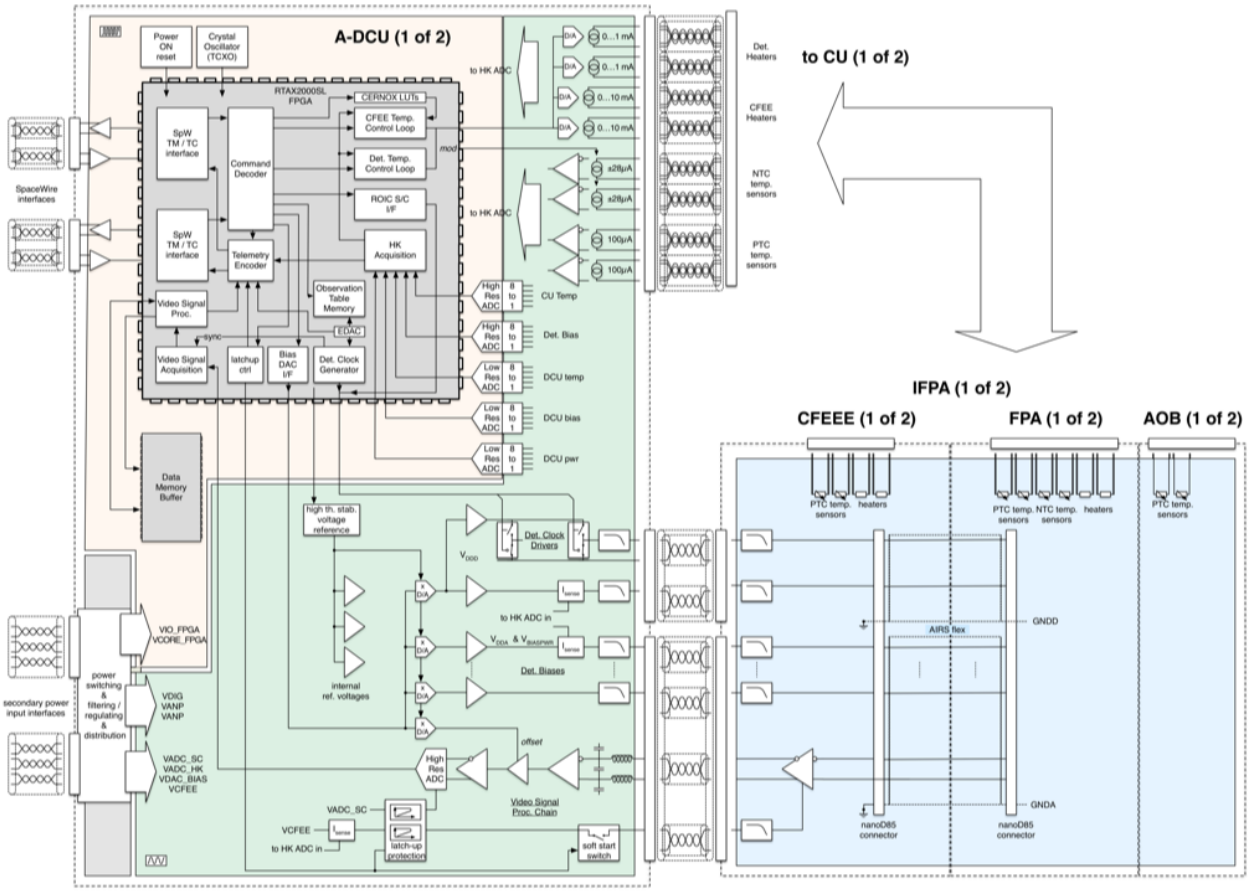

Figure 8: AIRS electrical architecture & A-DCU block diagram.

AIRS DCU electrical architecture defines six electrical interface signal families:

- Bidirectional digital interface (3-wire type)
- Detector clock output signal interface
- Analog signal input interface

- Power supply output interface
- Bias voltage output interface
- Thermal control

4. ICU/TCU DESIGN AND IMPLEMENTATION STATUS

The ICU is a warm unit residing into the SVM and it is based on a cold redundant configuration involving a Commanding and Data Processing Unit (CDPU) and a Power Supply Unit (PSU) along with a connecting backplane in order to provide internal data and secondary power supply (both analog and digital) IF. The ICU is in charge of managing the AIRS instrument by means of external electrical IF (data and secondary power lines), as the AIRS DCUs are hosted in an external dedicated box (A-DCU) whose electrical IF are cross-strapped to the nominal and redundant (PSU+CDPU) chains, as detailed in Figure 6 and Figure 9.
ICU is in charge of collecting scientific and housekeeping (HK) telemetries (TM) from the spectrometer and HK from the Telescope, the P/L Optical Bench (OB) - mainly temperatures readings - and other Subsystems (SS), thanks to a warm slave unit (TCU, Telescope Control Unit) serially interfaced to it. Science and HK telemetries are then forwarded to the S/C, for temporary storage, before sending them to Ground. TCU is also in charge of managing the secondary mirror (M2) refocusing mechanism, as described in Section 5.

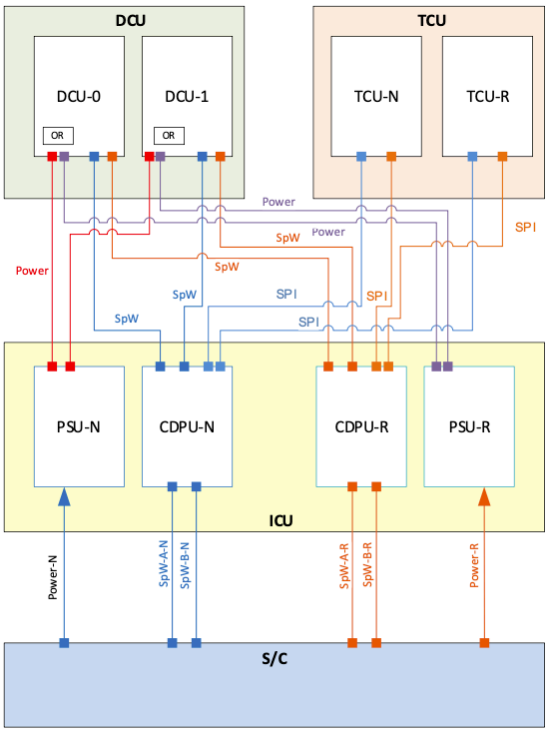

Figure 9: ICU electrical IF to the Spacecraft and to the Payload (A-DCU and TCU boxes).

4.1 Instrument Control Unit (ICU)

The ICU of Ariel is represented by an integrated box hosting two electronics chains working in cold redundancy. The main functions of the ICU are the following:

- Communicate with the Spacecraft via SpW links for Telecommands and telemetry.
- Provide the SpW data IF and secondary voltage levels to the AIRS Detector Control Unit.
- Collect scientific and housekeeping data from external A-DCUs and Telescope Control Unit (TCU).

- Compress scientific data and send them to the S/C (a customized lossless algorithm for spectrophotometric data, based on the heritage of the PLATO compression algorithm for photometric data only, is foreseen).
- Monitor the status of the Payload (TA, M2M, etc.) and provide it as telemetry.
- Perform FDIR procedures for the AIRS Instrument and at Payload level, exploiting the retrieved HK from the TCU.

The S/C provides nominal and redundant +28 V supply voltages to the ICU, which generates internal secondary voltages levels for its sub-modules and external secondary analog and digital voltages to the A-DCU only, as TCU generate them internally by means of its own PSU.
In particular, two isolated DC/DC converters supply the A-DCUs, each with multiple isolated outputs, namely:

- Isolated +4.5 V for the digital section.
- Isolated +7.1 V/-6.8 V for the analog section of both A-DCUs with a common return.

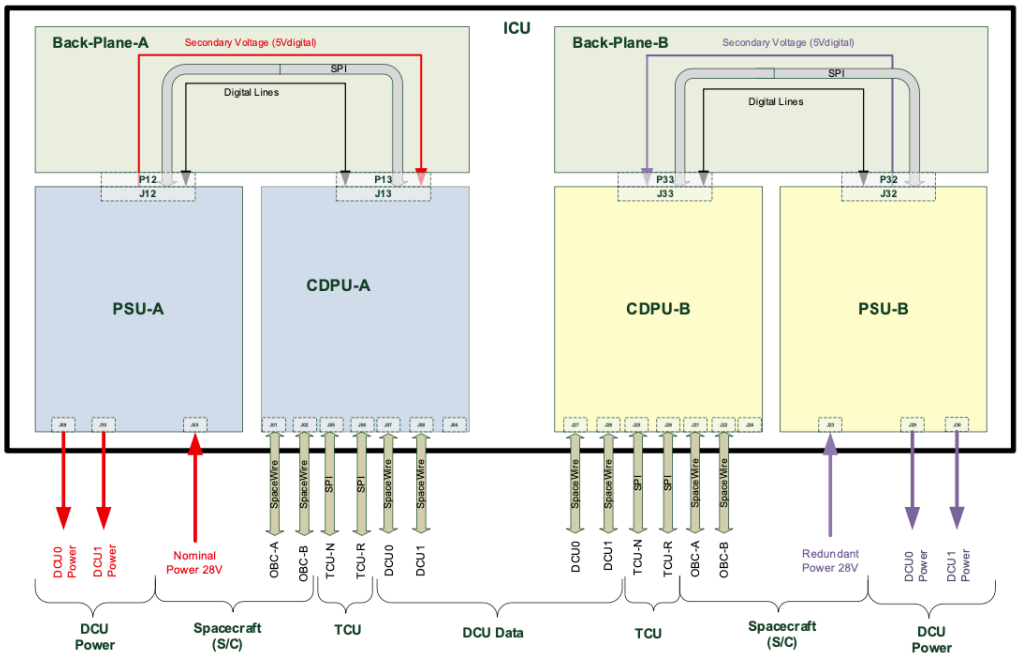

Figure 10: ICU electrical architecture.

The system architecture of ICU is detailed in Figure 10. Modules tagged as “A” are nominal and modules tagged as “B” are redundant and they accomplish the following functions:

- Nominal power supply Unit (PSU-A): it receives the +28 V from the S/C and provides the secondary supply voltages to the CDPU-A module and external A-DCUs.
- Nominal Commanding and Data Processing Unit (CDPU-A): it is the main data-processing module of the ICU. It is responsible for AIRS Instrument management, Payload thermal monitoring and M2M control and for interfacing the S/C for CCSDS Telecommands and Telemetry by means of 2 SpW links.
- Redundant power supply Unit (PSU-B): it receives the redundant +28 V from the S/C and it provides the secondary supply voltages to the CDPU-B module and A-DCUs. It is identical to PSU-A.
- Redundant Commanding and Data Processing Unit (CDPU-B): it interfaces the 2 redundant SpW links to the S/C and it is the identical to CDPU-A.

Each CDPU is internally connected with:

- PSU by Serial Peripheral IF (SPI) to acquire HK data (temperature, voltage and currents of the ICU) and by digital control/status signals to enable/disable power, select the channel to be acquired and readout protection status.

and externally to:

- A-DCUs via SpW for scientific data acquisition (from the spectrometer) and AIRS commanding
- TCUs via SPI for HK data acquisition at low data rate (maximum 10 kbps)

The CDPU board hosts an FPGA module and a CPU module, implementing the selected processor. The CDPU serves as the main control unit for the AIRS Instrument (through A-DCU) and TCU. It is based on the Frontgrade GR712RC System-on-Chip (SoC), featuring a dual-core Leon3FT CPU[†].

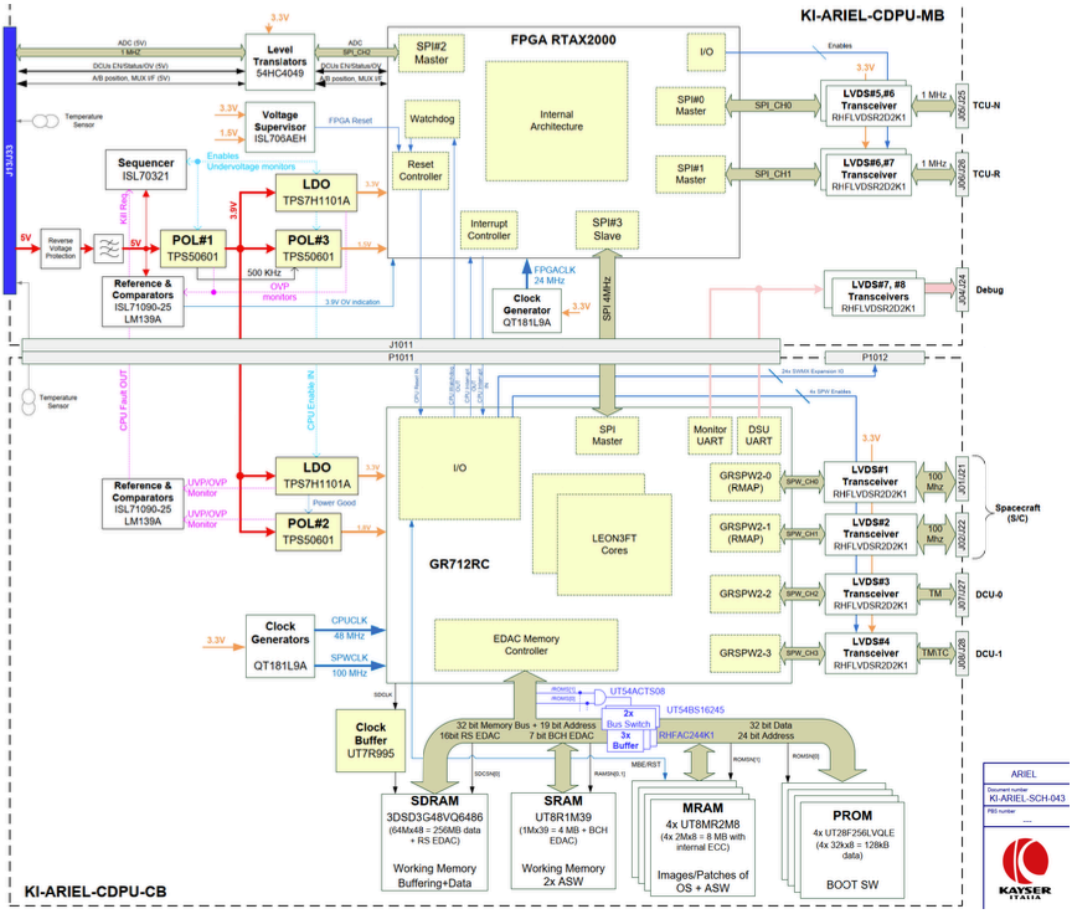

Figure 11: ICU CDPU block diagram (courtesy Kayser Italia).

The CDPU exploits 4 out of 6 embedded SpW links and other general-purpose peripherals, including SPI, memory controller, UART and GPIO controller, timers. To support the processor activities, the CDPU board is matched to an RTAX2K FPGA (refer to Figure 11), which provides additional interfaces for subsystems control, supports PL thermal monitoring by HK data acquisition, manages M2M HK and implements the SPI IF to TCU for a quick and simple HK retrieval task from both TCU and external subsystems. The CDPU board includes 4 MB of SRAM working memory, 8 MB of MRAM memory to store at least 2 versions of the Application Software (ASW) one of which to be loaded at boot

[†]The same processor has been selected for controlling the Fine Guidance System, in order to exploit commonalities and synergies between the two Instruments On-Board SW.

in the working memory and 256 MB of SDRAM as buffering memory to support the working memory and for temporary data storage and, finally, 128 kB of MROM memory to store the Boot Software (BSW).

The FPGA module communicates with the PSU to acquire housekeeping signals, status and to command it for the A-DCUs switching on/off. The electrical IF is implemented by means of voltage buffers: the selected part is ESCC 9401/037/02F from ST Microelectronics, a HCMOS Hex Buffer/Converter with fully buffered inverted outputs. In detail, the interfaces managed by the FPGA are:

- A complete Master SPI interface, designed to operate at 1 MHz of SCLK at board level (maximum 2 MHz), dedicated to the slave ADC implemented in the PSU;
- A Multiplexer Address and Command interface, in order to drive the MUX provided in the PSU to extend the ADC number of channels;
- A-DCU enable and status signals for the PSU, using the CPU GPIO;
- An A/B select input from the back-plane, with pull-up, acquired by the FPGA and available for the CPU software through a dedicated status bit/register.

The SW onboard the Ariel ICU [12] [13], managing AIRS and TCU, is based on the following three components:

1. *Boot Software*: it is installed on the PROM (128 KB) of the ICU CDPU board and allows loading/deploying the ICU Application Software to RAM. It is a critical (Category B) and low complexity SW.
2. *Basic Software*: Basic I/O SW, Service SW & Peripheral Drivers: it is used by the Application SW and depends on the selected Real Time Operating System (RTOS).
3. *Application Software (ASW):* it is the actual ICU-AIRS-TCU control software and implements:
    a. the AIRS and TCU handling functionalities,
    b. the instrument health monitoring,
    c. the FDIR procedures handling and
    d. the interface layer between the S/C and the instrument.

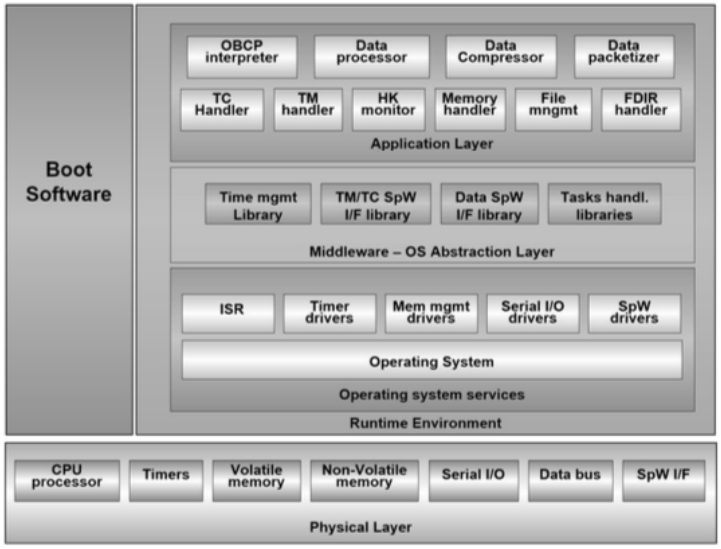

Figure 12: ICU CDPU SW layers

The AIRS Data Processing and Compression Software is part of the ICU ASW as well and implements all the necessary on-board scientific data pre-processing functionalities, preliminary to the lossless compression task. ICU to A-DCU internal communication is based on a simplified protocol over SpaceWire, lighter and similar to the RMAP

one, already adopted on VIS instrument on-board EUCLID. Being the ICU ASW a patchable real time SW it can be assigned to criticality category C (according to ECSS standard criticality level definition). The ASW patching functionality will be implemented at Boot SW level. At that level it will be possible, through the memory management service, to patch tables and, more in general, data. It will not be possible to patch the ASW at runtime on the ICU operating CDPU+PSU chain, while it shall be possible on the redundant chain once switched on and operating in Boot SW mode.

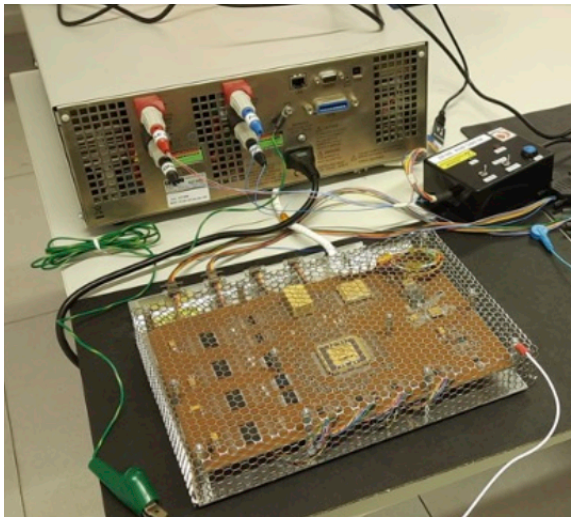

Figure 13: ICU CDPU EM grade subject to BLT at INAF premises.

ICU EM CDPU (refer to Figure 13) already underwent a first Board Level Test (BLT) campaign and it has been delivered, along with a preliminary PSU version, to INAF as the Scientific Institute in charge of unit responsibility and Application SW (ASW) development, integration, test and validation. Boot SW (BSW) and drivers (BSP – Basic Support Package) are instead in charge of Kayser Italia, as well as the overall HW development and test.

Finally, the ICU box (MD – Mechanical Dummy, EM – Engineering Model and AVM – Avionic Validation Model) mechanical design is shown in Figure 14. It differs with respect to the following models owning to the ICU Model Philosophy (EQM – Engineering Qualification Model and PFM – Proto Flight Model) as they will host 5 M6 IF bolts to the S/C per side in order to face the expected mechanical stress at launch related to the Ariane 6.2 rocket.

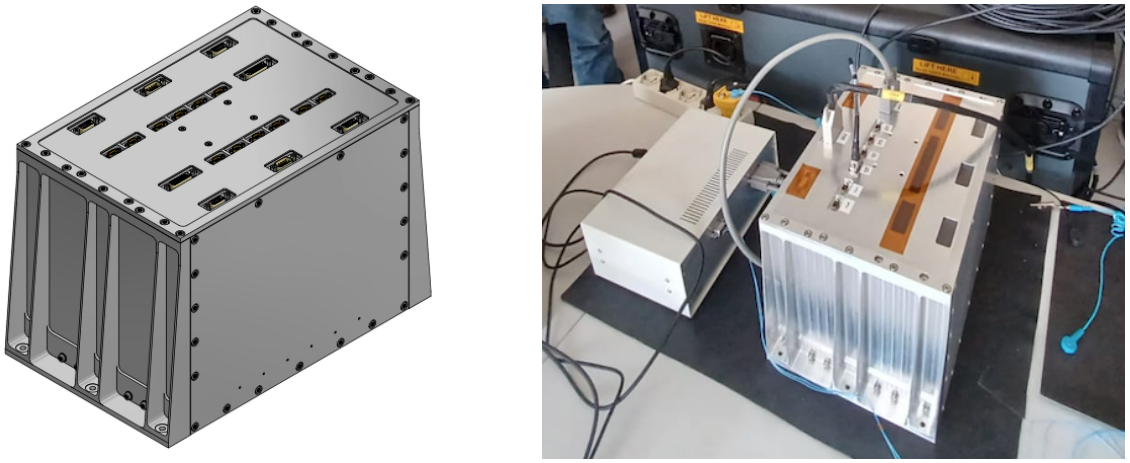

Figure 14: ICU mechanical enclosure. Left: 3D MD and EM/AVM CAD design. Right: EM box hosting a single chain along with its debugging box and SIS – Spacecraft IF Simulator (on the background) at INAF premises.

ICU MD was developed, tested and delivered to the S/C Prime Contractor (ADS) in Autumn 2023 while, presently, both the EM and AVM models are under assembly (PSU) and test (PSU, CDPU) at ICU Prime Contractor (Kayser Italia) premises in Livorno, Italy.

4.2 Telescope Control Unit (TCU)

The Telescope Control Unit drives the M2M and monitors the PLM cryogenic temperatures. The system is divided in three boards:

- CTS: the Control and Thermal Sensing board, where the controlling FPGA and the sensing chain to measure the PLM temperatures are located.
- M2MD: the M2M Driver, that controls the stepper motors that move the M2M using a current control approach.
- PSU: the Power Supply Unit, that adapts the primary bus supply voltages to the ones needed by the other two boards.

There is a fourth board, the back-panel, that interconnects them. Finally, the chassis protects the boards from mechanical stress and reduces the internal radiation level. The different components are represented in Figure 15.

Figure 15: TCU internal components and chassis.

The CTS, Back-Panel and unit Chassis are designed by the IEEC while the M2MD and the PSU are designed by SENER.
The system is controlled by a Microchip FPGA of the RT ProASIC 3 family. This family is Radiation Tolerant and flash-programming based. This has been possible thanks to the expected radiation level inside the TCU chassis, and a thorough thermal analysis that reduces the temperatures reached by the FPGA, ensuring that it will work properly throughout the mission. Finally, a Triple Modular Redundancy (TMR) strategy will be followed to minimize radiation effects, especially on the M2M driver, as any failure can potentially jeopardize the Ariel telescope refocusing functionality.
The CTS includes also HK channels for the internal temperatures, and the voltages and currents provided by the PSU. This approach shall help to identify and determine the sources of possible issues while testing on-ground, or once space-borne. The FPGA is also expected to include self-test sequences. This approach was already used in Solar Orbiter PHI Instrument, helping to better characterize different issues while testing.
The M2M control and the PLM thermal monitoring functionalities are presented in the next subsections.

4.3 M2M control

The M2M is a mechanism that must be tested at laboratory and cryogenic temperatures, as it will be assembled in the TA. This change in temperatures affects the characteristics of the stepper motors. For this reason, a constant current

control driver is used, which ensures the proper torque of the motor at any working temperature. The position of the motor is confirmed by the use of switches that are activated on each turn of the motor.
To minimize the changes of temperature associated to the power consumption of the motors, only one of them is used at a time. As a result, the control hardware is replicated for each motor, while the firmware that controls it is multiplexed. This reduces also the resources from the FPGA when implementing the TMR strategy.

4.4 PLM thermal monitoring

The CTS includes the Thermal Sensing Module that measure the 37 cryogenic temperatures on the different points of the TA. This is done using a four-wire configuration, with a fully differential measurement, and driven with positive and negative current to minimize Seebeck effects. The bias currents are very low, on the order of micro amperes. For this reason, a Howland Current Source (HCS) is used. The HCS can be controlled by a Digital to Analog Converter (DAC). To minimize errors, the voltages on the single probe and the voltage that drives the HCS are measured by a 32 bits ADC. This allows to compensate part of the errors.
As there are 37 sensors on the TA, it is necessary to multiplex the signals to reach every individual sensor. Each multiplexer introduces a new uncertainty associated with the leakage current. For this reason, each multiplexer includes a calibration resistor on one channel that allows to have an estimation of this leakage current. The resistor value is measured through the same chain as the external sensors, allowing to compensate it.
The resulting system has the 37 external channels for the TA sensors, plus 11 internal calibration channels. With this configuration, the expected precision in the worst-case scenario is around 11 mK, that shall be added to the sensor's uncertainty. The FPGA firmware (FW) does not include any processing capability, as the HK data are expected to be delivered to the ICU, forwarded to the S/C as CCSDS TM and, then, un-packetized and processed on-ground.

5. FGS DESIGN AND IMPLEMENTATION STATUS

The Fine Guidance System is an opto-electronic instrument working as a visible photometer and a low-resolution near-infrared (NIR) spectrometer. Apart from providing a high precision astrometry and photometry of the targets for complementary science, its fundamental task is to ensure centering, focusing and guiding of the satellite.
From an engineering point of view, FGS consists of a cold part, a warm one, and the connecting harness, similarly to AIRS. Two types of harness are adopted as in AIRS: a cryo-harness and a typical warm harness.
The cold part includes the detection chain units: the FGS Optical Module (FOM) with two Focal Plane Modules (FPM) and a Focal Plane Electronics (FPE) box. Both FPM and FPE are part of NASA/JPL contribution to Ariel (CASE - Contribution to ARIEL Spectroscopy of Exoplanets). The warm section includes only the FGS Control Unit (FCU), hosting two Detectors Control Units (F-DCU) provided by Italy through OHB-I, as described in the following.

5.1 FGS Detectors and cold front-end electronics

The cryogenic detector system for the FGS is composed of H2RG [15] and packaged [16] SIDECAR ASIC inherited from flight spares made for the Euclid NISP instrument [17]. New thermal-mechanical hardware was designed to adapt the Euclid hardware for the FGS Ariel interface requirements. Also, new firmware developed to operate the H2RG for fine guidance control of Ariel. The driving requirements for the firmware are to sample only the optically exposed detector area and the reference pixels and to achieve a frame rate of 20 Hz. These drove definition of stripe mode and pixel rate of 125 kHz with line reset.

5.2 FPM – Focal Plane Module

The Focal Plane Module (FPM) is specially designed mechanical hardware to allow kinematic mounting of the H2RG to the FGS optics and box and also temperature stabilization of the H2RG during operation with minimal control heater power. H2RG performance was tested for Ariel use in the range 62-68 K with ASICs running the new firmware and flight designed 42 cm long flex cable run. The firmware is loaded onto the ASICs after power up and handle set up, image acquisition and data handling of the H2RGs. The detected quantum efficiency was measured over a range 450-2300 nm and shown to meet requirements for the optical and infrared bands of the FGS. Each FPM includes a nominal and redundant heater and Cernox resistive thermometer to be used as temperature control of the H2RG. A total of 4

flight quality FPMs have built and tested to mount to the two detector positions on the flight FGS optics box. The flight FPMs are scheduled for delivery to CBK in fall of 2024.

5.3 FPE – Focal Plane Electronics

Low thermal conductance flex cables [18], each a total length up to 42 cm, connect the H2RG to the SIDECAR ASICs located outside of the main Ariel instrument cavity. Each flex cable is divided into two segments, the cryogenic flex cable (CFC) and FPE Input Cable (FPEIC). The CFC connects to the H2RG on the FPM and then to the FPEIC at a cut-out at a bulkhead on the optical bench. The cut-out on the bulkhead provides mechanical support on the middle of the cable and prevents light leaks into instrument cavity. Each FPEIC connects to one of two ASICs mounted inside the Ariel cryogenic focal plane electronics box (FPE), as shown in Figure 16. The FPE maintains the ASICs at the nominal operating temperature of 137 K and above the minimum temperature qualified for the Euclid project (>130 K). Heat from the ASICs and thermal control systems are radiated to deep space via black paint on the top of the FPE which is co-planar with the main Ariel instrument radiator. Thermal isolation of the FPE from the Ariel telescope optical bench at 50-60 K is provided by fiberglass struts. Additionally, the struts and mechanical structure of the FPE box were required to have a high stiffness to achieve a lowest vibrational mode >140 Hz. The implement design has a lowest mode >170 Hz as verified in vibration test. Heater and thermometers are included in the FPE for two types of temperature control. One type is for fine temperature control <100 mK p-p stability and is operated by the warm instrument electronics. The other is a survival control to be operated by the spacecraft to ensure the ASICs are always above 130 K when the instrument is off or in some other off nominal condition safe hold condition. The flight FPE and flex cables are currently in final cryogenic testing and scheduled for delivery to AMC in the fall of 2024.

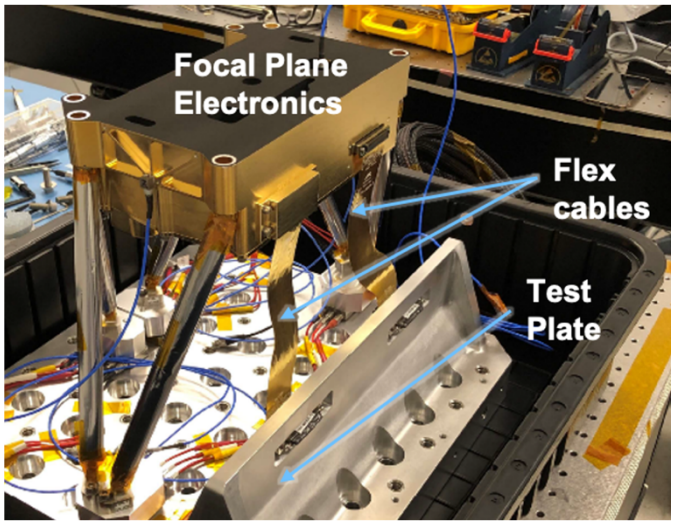

Figure 16: Focal plane electronics (FPE) and (2) FPEIC connected to ASICs within the FPE on one side and to a mockup of the bulkhead pass through on a test plate used for vibration testing.

5.4 FGS Detector Control Unit (F-DCU)

The F-DCU manages the FGS detector system composed by the front-end electronics SIDECAR ASIC and the HawaII-2RG (H2RG) HgCdTe near infrared detector, as described in the previous paragraphs. The F-DCU and SIDECAR communication interface consists in two sections, an 8-bit parallel “science data” interface (using 8x LVDS lines) with adaptive sampling, and the “tele-command and telemetry” (TMTC) interface (using a serial line).
Science data is generated by the SIDECAR when commanded by the F-DCU to initiate an acquisition, and the F-DCU receives from each SIDECAR from 1 to 4 stripes composed by a number of consecutive complete rows (2048 pixels each) at 16 bits. The F-DCU has an image processing capability to extract up-to two crop zones from the stripes, and implements an image buffering by means of an external SDRAM memory buffer (1 Gbit) EDAC protected. The SDRAM memory is also used as temporary buffer for DMA operations to the mass memory board. Data processing

(image cropping plus housekeeping extraction present in the science data packet) is implemented in a reprogrammable RT ProAsic FPGA.
Command reception from the Data Processing Unit (DPU), interpretation and translation to a SIDECAR are provided by the F-DCU. As well as a set of registers and memory areas to allow the DPU to monitor, command and configure the F-DCU and the SIDECAR. This approach is adopted to grant the maximum flexibility to the FGS application software.
The electrical interfaces of each F-DCU are:

- +28 V Primary Power from PSU (Main + Redundant).
- +5 V Secondary Power from PSU (Single input).
- Secondary Power to SCE.
- Science Data from SCE.
- TM/TC from/to SCE.
- SpW I/F from/to DPU (Main + Redundant).
- Clock from DPU (Main + Redundant).
- SYNCH from DPU (Main + Redundant).
- Internal voltage monitors to DPU.

The F-DCU provides to the SIDECAR, using 3 insulated power subgroups, 5 very low noise isolated secondary power supplies: two analog (VDDA of +3.3 V and VDDA sense), two digital (V3P3 of +3.3 V and V2P5 of +2.5 V) and a voltage reference (V_{Ref} of +3.3 V ± 0.05%) generator with power sequencing, voltage adjustment via DAC and return current isolation, overvoltage and overcurrent protections. It also provides two power supplies (VDDIO of +1.65 V, VSSIO of +0.9 V) to the communication interface with the SIDECAR. The nominal power dissipation on loads in this configuration is 270 mW. Due to load regulation requirements of the analog section of the SIDECAR, the post regulator of the analog power conditioning section is provided with load sensing to ensure accurate regulation of the VDDA voltage at SIDECAR board.
The F-DCU board is controlled through a cold redundant SpaceWire link (using remote memory access protocol - RMAP), providing science data though the same link with autonomous SpW packet transmission (not RMAP) at a frequency of 60 MHz with a maximum data rate of 48 Mb/s.
The DPU provides to the F-DCU two cold redundant 40 MHz clocks on LVDS electrical levels, and the SIDECAR clock is derived from the clock received from the DPU by division. It also provides to the F-DCU two cold redundant synchronization signals on the LVDS electrical levels used to trigger the detector synchronization function.
A picture of the F-DCU board showing the disposition of the components can be seen in Figure 17.

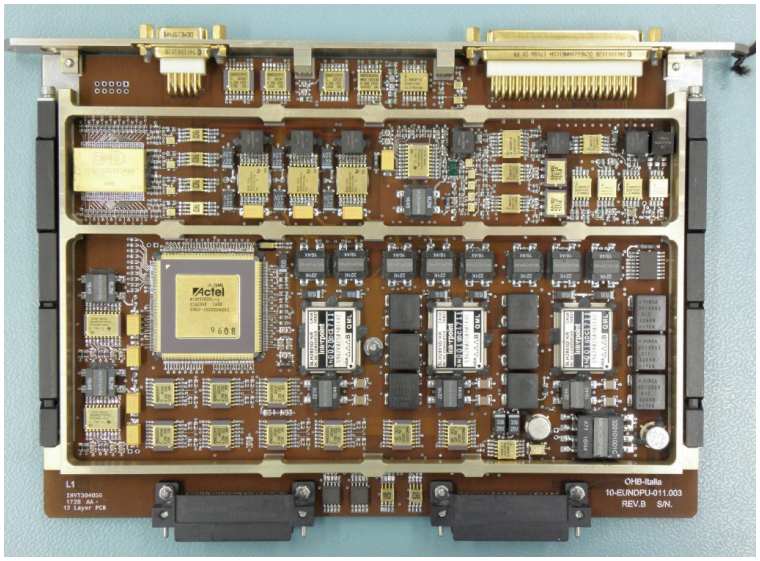

Figure 17: Top view of the F-DCU board EM model showing the components disposition i.e. A/D converter (top left side) RTPROASIC FPGA (middle left). SIDECAR I/F (top right connector), FPGA I/F (top left connector.) and backplane I/F (bottom connectors) are shown. Picture courtesy OHB-Italy (designer and manufacturer).

5.5 FGS Control Unit (FCU)

The FGS FCU comprises several subsystems: two Detector Control Units (F-DCUs 1 and 2), two Data Processing Units (DPU Main and Redundant), one Thermal Control Unit (FGS-TCU), two Power Supply Units (PSU Main and Redundant), and a Backplane PCB. The DPU and PSU operate using a cold redundancy scheme, which means that only one of them is active at any given time. Meanwhile, the F-TCU employs a combination of warm and cold redundancy, and both F-DCUs function in warm redundancy mode, allowing to be active simultaneously.

The DPU serves as the main control unit for the entire FGS. It is based on the Aeroflex GR712RC System-on-Chip (SoC), featuring a dual-core Leon3FT CPU. The DPU incorporates six SpaceWire codecs and various other general-purpose peripherals, including memory, UART, GPIO controller, and timers. To support the processor, the DPU integrates an RT ProAsic 600L FPGA, which provides a memory-mapped interface for subsystem control, collects housekeeping data, supports thermal control loops, manages power lines, and implements over-voltage protection. The DPU includes 16 MB of SRAM operating memory, 2 MB of MRAM memory to store the Application Software image, and 128 kB of MROM memory to store the Boot Software. Communication with the spacecraft occurs via the SpaceWire interface.

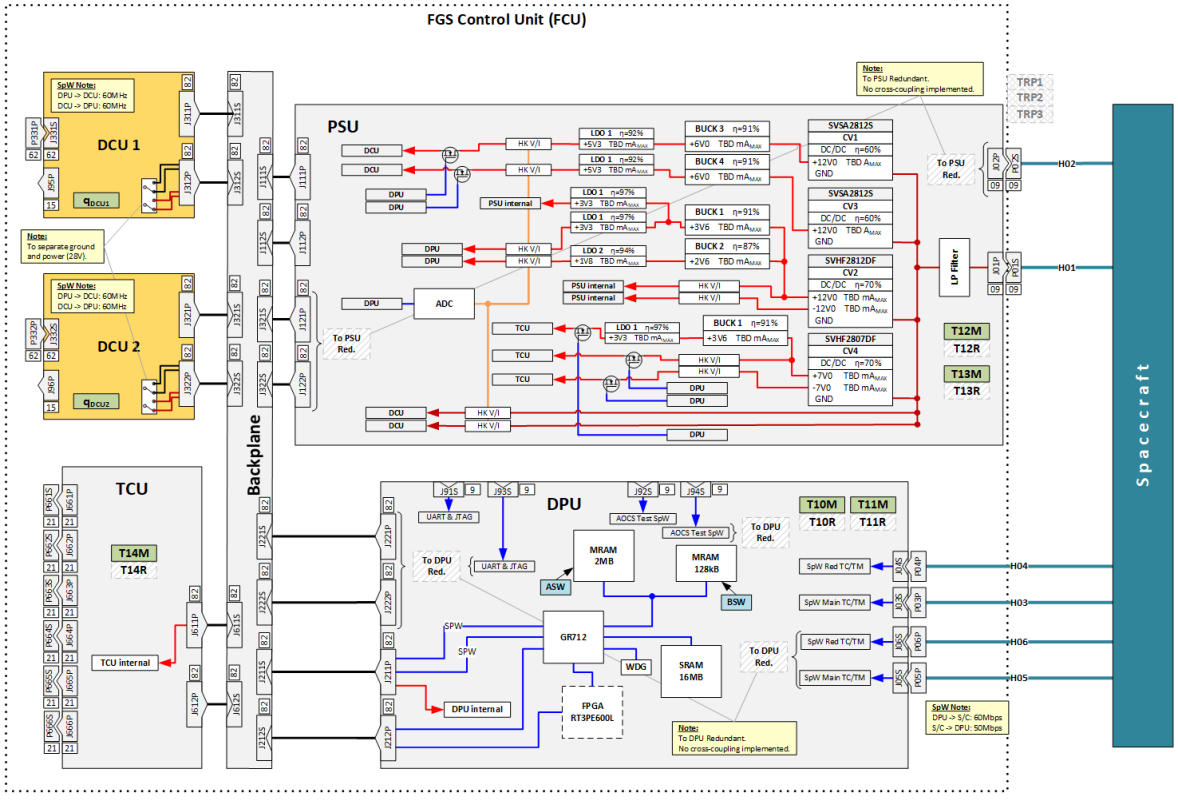

Figure 18: FCU concept and detailed block diagram.

The F-TCU plays a critical role in the FGS. It measures temperatures from the FPM, FPE, and FOM modules, ensuring their stability. The temperature stabilization relies on readings from ten independent Lake Shore Cernox CX-1080 temperature sensors (five main and five redundant). Additionally, operating heaters are strategically placed on the FPM and FPE modules. These heaters operate in a redundant configuration, with a total of six independent heaters. The control loop responsible for temperature stabilization is implemented in the DPU FPGA. The F-TCU is divided into main and redundant sections, and both are powered by the PSU. However, only one of the sections actively controls the heaters at any given time.

The PSU comprises three subsystems: power distribution, housekeeping, and power switches. The power distribution section includes an input low-pass filter, a set of three converters (SVSA2812S, SVSA2812DF, SVSA2807DF) that

transform the input +28 V into intermediate voltages, and a combination of LDOs (TPS7H1101-SP and TPS7A4501-RHA) and buck converters (SPPL12420RH) that generate secondary voltages within a range of 1.8-7 V (including complementary negative voltages). Additionally, it supplies the +28 V power line to the F-DCUs. The housekeeping subsystem monitors voltage and current levels on output power lines and retrieves data from internal temperature sensors. The PSU incorporates eight output switches, which are controlled by the DPU to enable or disable the F-DCU and F-TCU units.

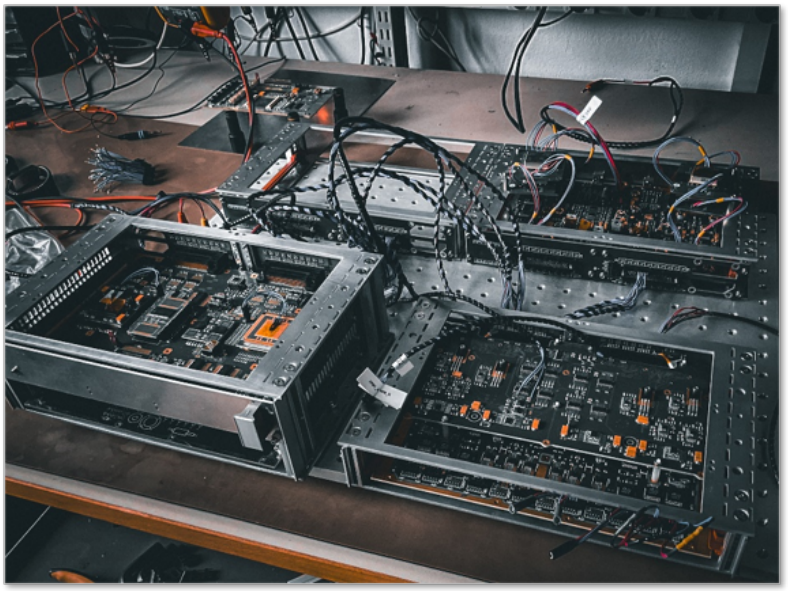

Figure 19: FCU pre-EM model assembly at CBK premises

The backplane board serves as an electrical connection hub, linking all FCU boards together. Specifically, it contains fourteen CMD082EFEY38 connectors.
Finally, the FCU Box encloses all the FCU subsystems. The FCU mechanical parts are based on aluminum 6061 and/or 7075. To assure low electrical resistance, all metal surfaces have a coating. Additionally, the external surfaces are black painted. Figure 20 shows the FCU box model.

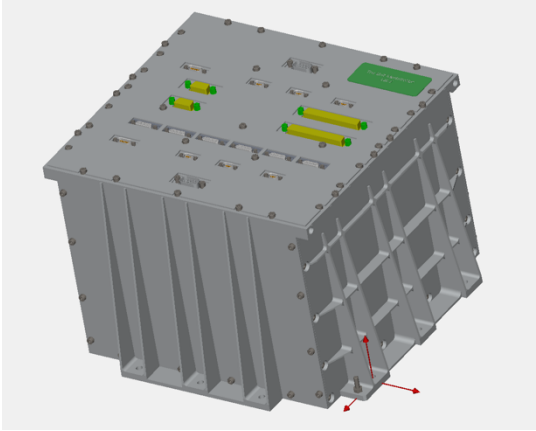

Figure 20: FCU box CAD model.

The FGS flight software (FSW) [19] comprises two main components: Boot Software (BSW) and Application Software (ASW). Upon power ON, the DPU executes the BSW. The BSW performs several critical tasks, including initializing the CPU, conducting health checks on the instrument, and by default, executing the ASW. However, in emergency situations, a telecommand from the spacecraft can halt the execution of the ASW, leaving the BSW in Standby mode. In

the Standby state, ground operators have the capability to perform memory loads or dumps, which can be useful for post-mortem investigations if the instrument fails to start properly.

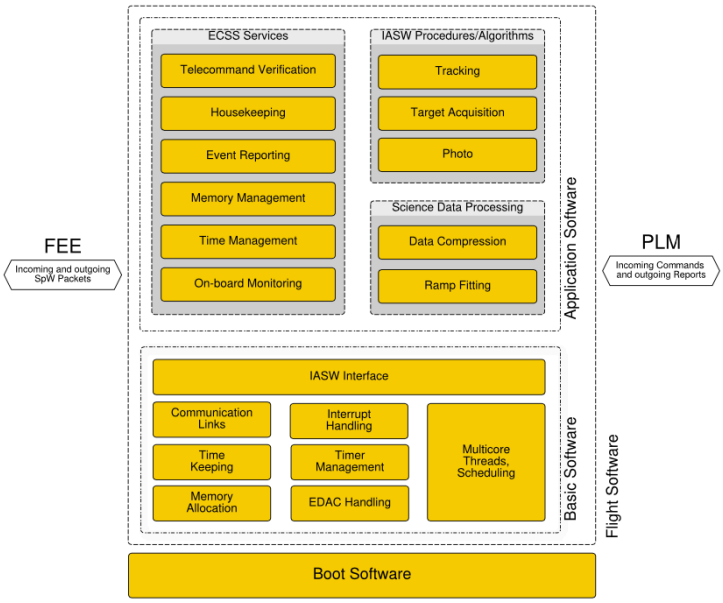

Figure 21: Hierarchical layout of the Ariel FGS software.

The Application Software (ASW) consists of two main components: Instrument Basic Software (IBSW) and Instrument Application Software (IASW). The IBSW serves as a layer that provides operating system functionality and functions for controlling the hardware. On the other hand, the IASW represents the top software layer, implementing all the necessary algorithms and procedures required to operate the instrument.

6. ACS DESIGN AND IMPLEMENTATION STATUS

As anticipated in Section 2, an Active Cooler System (ACS) is being used to cool both channels, CH0 and CH1, of the AIRS instrument. The Ariel Telescope Optical Bench, upon which AIRS and the FGS instruments are located is passively cooled to 50–55 K, however the AIRS detectors require operation at a lower temperature (approximately 40 K) and the purpose of the ACS is to provide the additional cooling power needed.

The ACS is a closed cycle Joule-Thomson (JT) mechanical cryocooler using neon as the working fluid. A schematic of the ACS is shown in Figure *22* and a system definition and breakdown are given in Table 1. The ACS provides active cooling at the cold tip thermal interface by performing a Joule-Thomson expansion of the working fluid across a restriction, in this case an orifice. The cooler is operated sub-critical, collecting the liquid produced after expansion in a reservoir such that the heat exchanger return-line pressure above this reservoir determines the temperature.

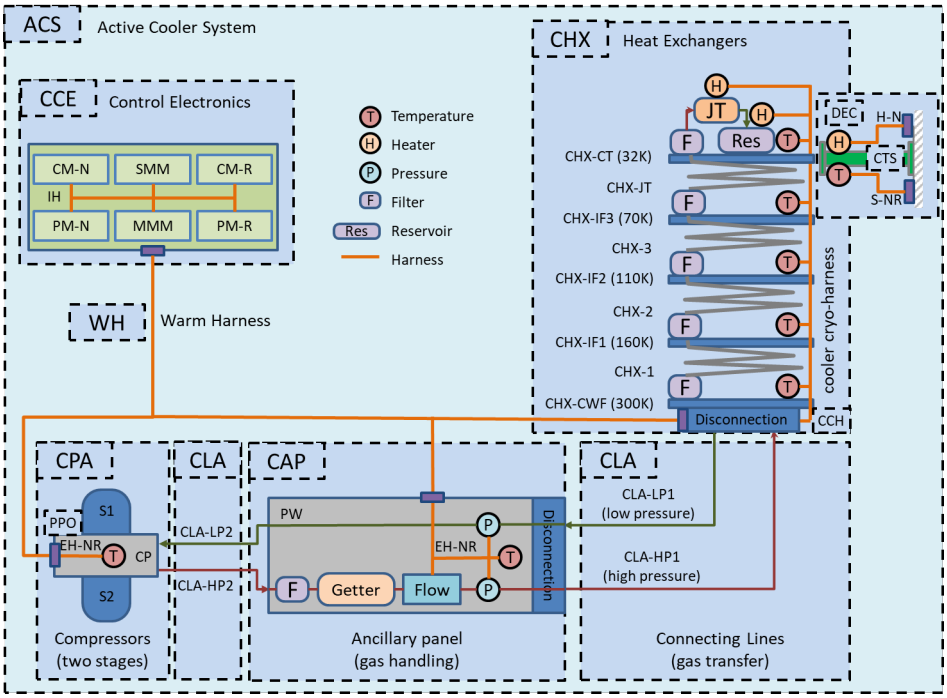

Figure 22: Active Cooling System Schematic

PRODUCT CODES
WH – Warm Harness
WH-ACS – ACS warm harness
ACS – Active Cooler System
CCE – Cooler Control Electronics *CCE-CM-N – control module (nominal), CM-R (redundant)* *CCE-PM-N – power module (nominal), PM-R (redundant)* *CCE-SMM – sensor MUX module* *CCE-MMM – motor MUX module* *CCE-IH – internal harness*
CPA – Compressor Assembly *CPA-S1 – Compressor Stage 1* *CPA-S2 – Compressor Stage 2* *CPA-CP – CentrePlate and interface* *CPA-EH-NR – External sensor Harness (nominal and redundant)*
PPO – Position sensor pre-amplifier
CAP – Cooler Ancillary Panel *CAP-PW – pipework and baseplate* *CAP-EH-NR – external sensor harness (nominal and redundant)*

CLA – Connecting Line Assembly
CLA-HP1 – CAP/CHX high pressure connecting line
CLA-LP1 – CAP/CHX low pressure connecting line
CLA-HP2 – CPA/CAP high pressure connecting line
CLA-LP2 – CPA/CAP low pressure connecting line
CHX – Cooler Heat Exchanger Assembly
CHX-CWF – Heat Exchanger warm flange (disconnection box)
CHX-IF1 –Heat Exchanger VG1 interface
CHX-IF2 – Heat Exchanger VG2 interface
CHX-IF3 – Heat Exchanger VG3 interface
CHX-CT – cold tip interface
CHX-1 – Heat Exchanger #1
CHX-2 – Heat Exchanger #2
CHX-3 – Heat Exchanger #3
CHX-JT – Joule-Thomson heat exchanger
CCH – Cooler Cryoharness
CCH-N – Cooler Cryoharness (nominal)
CCH-R – Cooler Cryoharness (redundant)
CTS – Cold Tip Support (To TOB)
DEC – Decontamination hardware
DEC-S-NR – Sensor Harness (nominal and redundant)
DEC-H-N – Heater Harness (nominal), H-R (redundant)

Table 1. ACS System Definition and Breakdown (to be read in conjunction with Figure 22).

The compressors (CPA) circulate the neon gas around the system by a set of reciprocating linear motor compression stages, with an arrangement of reed valves and buffer volumes, to produce a dc flow through the Joule-Thomson orifice whilst maintaining the pressure ratio across it. Two compression stages in series (CPA-S1 and CPA-S2) are needed in order to produce the required high and low pressures.

The gas must be pre-cooled prior to the Joule-Thomson expansion taking place, there are three pre-cooling stages available from the spacecraft V-groove radiators and, to optimize the heat rejected at these pre-cooling interfaces (CHX-IFn), counter-flow heat exchangers (CHX-n) are used between them.

The ancillary panel (CAP) carries gas handling and measuring equipment, as well as particulate filters and a reactive getter to ensure gas cleanliness, which is critical to the long-term operation of the cooler.

The disconnection plates and connecting pipework (CLA) allow the system to be separated into several pieces to aid integration. This allows the heat exchanger assembly to be delivered and integrated with an instrument independently from the CPA and CAP, with a final purge, gas cleaning and fill procedure being carried out after installation of the CLA to re-connect the CPA/CAP to the CHX.

The cooler is controlled by a set of drive electronics (CCE) which perform all commanding and controlling functions as well as providing the electrical input power for the compressors and returning the cooler housekeeping data.

As can be retrieved from Figure *22* electrical and electronic elements are present in all the major mechanical sub-systems (CPA, CAP and CHX), which are powered and controlled by the CCE and its associated harnessing. These sub-systems are described in more detail below.

6.1 Cooler Control Electronics (CCE)

The Active Cooling System (ACS) is operated through a dedicated Cooler Control Electronics (CCE) unit. Figure 23 depicts its mechanical design along with the external electrical IF hosted by connectors. The CCE contains the power conditioning for the compressor motors, telemetry acquisition for each of the unit within ACS, as well as telemetry/telecommand interface to the S/C OBC implemented on MIL-BUS protocol. The main purposes of the CCE are to control the compressor motors with stable amplitude, and to minimize the exported micro-vibrations produced by the motor pistons.

The motor drive waveforms are generated by means of Direct Digital Synthesis (DDS), which is driven by an FPGA. This enables efficient and robust implementation of control algorithms for the motor drives in digital domain. The CCE implements two types of closed-loop controllers: one for controlling the CPA piston position amplitude, and one for micro-vibration reduction.

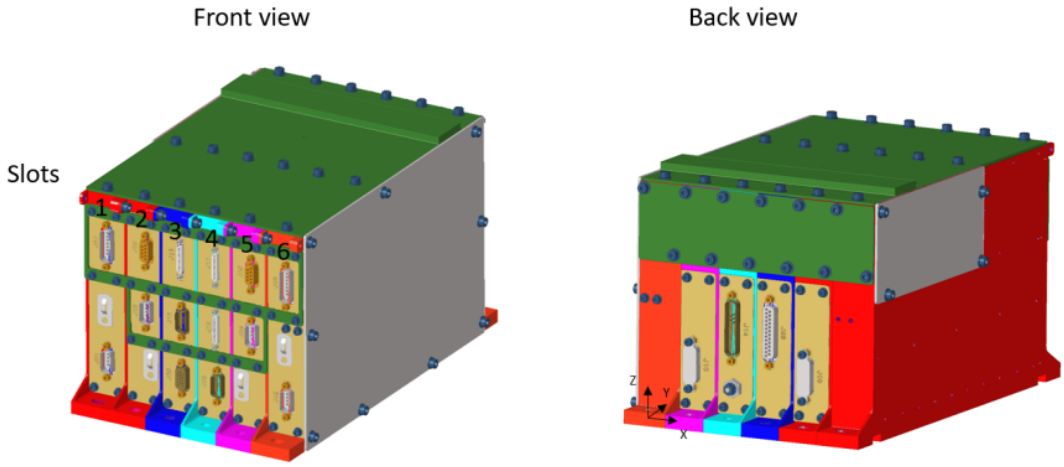

Figure 23: CCE box CAD design.

The position information from the motor pistons is retrieved via Position Pick-Off (PPO) mechanism, which is based on capacitive De-Sauty bridges. The obtained position amplitude is used as feedback for PI controllers that steer the fundamental amplitudes of the drive waveforms. This allows precise regulation of the piston amplitudes for each of the two motors individually, which in turns allows controlling the cooling power of the ACS, as well as constraining the piston amplitude within safe range upon pressure changes in the cooling system.

In addition to position control, the CCE is capable of mitigating the exported micro-vibrations from the CPA by distorting the drive waveform of one of the two motors. The CCE measures the forces exported from the CPA and processes the signal in digital domain to obtain the phases and gains of the harmonic series of the motor drive frequency. Based on this information, the micro-vibration algorithm generates the distorted drive waveforms for the motors so that the forces resulting from mechanical imbalances of the pistons are effectively cancelled on the piston axis for each of the controlled harmonic.

The CCE high-level electronics block diagram is shown in Figure 24.

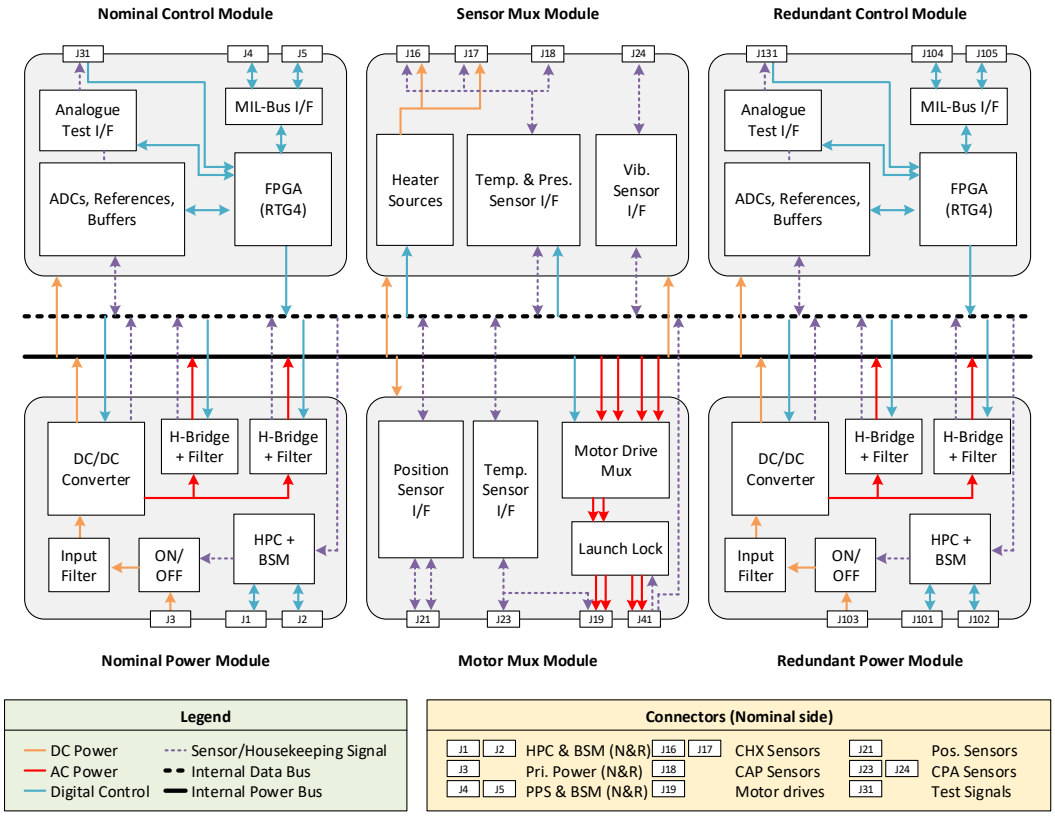

Figure 24: CCE Overall Electronics Block Diagram.

As shown in the diagram, CCE consists of six modules, four of them being redundant (N&R control and power modules) and two non-redundant (motor and sensor mux). Detailed description of the different modules is given in the following subsections.

6.1.1 Power Module

Power Module interfaces the Ariel CCE to the Power Conditioning and Distribution Unit (PCDU) and is primarily responsible for generating internal voltages for the CCE, as well as the motor drive signals for the two motors in the Compressor Assembly (CPA) with H-Bridges.

The power module also provides interfaces towards nominal and redundant On-Board Computer to switch the CCE on or off via High Power Commands (HPC), to monitor the status of the launch lock and CCE ON/OFF status via Bi-level Switch Monitor (BSM) interface.

6.1.2 Control Module

Control Module contains the main FPGA and is therefore responsible for all data processing and control within the CCE. The control module provides telemetry and telecommand interface to the OBC via MIL-STD-1553 bus (A and B).

Sensor data from the mux modules, as well as internal analogue telemetry, are digitized on the Control Module via Analog-to-Digital Converters (ADC) connected to the main FPGA. All control algorithms, telemetry processing, state machines and control signal generation reside in the FPGA. The control signals drive the H-Bridges on the power module to generate the drive signal for the two motors within CPA.

The analogue test output signals are also provided via this module, either by directly routing the analogue signal to the test connector, or in the case of position signals, synthesized in the FPGA.

6.1.3 Sensor Mux Module

Sensor Mux Module is responsible for interfacing the CCE to the temperature and pressure sensor interfaces within Cooler Ancillary Panel (CAP) and Cooler Heat Exchanger (CHX) modules, as well as the vibration sensors within the CPA. This module contains the EMI filters, multiplexers, first amplifier stages and excitation signal sources for the interfaced sensors. It is therefore also the common interface to multiplex the non-redundant external interfaces to the nominal and redundant Control and Power modules within CCE.

6.1.4 Motor Mux Module

Motor Mux Module interfaces the CCE to motor drive and temperature sensor interfaces, as well as position sensing interfaces (via PPO pre-amplifier) within the Compressor Assembly (CPA). Launch locks, connected to the motor drive signals, are also contained within this module.

The motor drive signals, which are generated on the nominal and redundant power modules, are multiplexed to the two non-redundant motors via relays. Similarly to the Sensor Mux Module, this module contains the EMI filters, multiplexers, amplifiers and excitation sources for the sensors within CPA (including PPO), and the module splits these interfaces to the nominal and redundant control and power modules.

6.2 Cryocooler Compressor Assembly (CPA)

The CPA developed and built for the Ariel Technology Demonstration Activity is shown in Figure 25 (along with the CAP). The CPA mechanisms are built around moving coil linear motors, which are driven by sinusoidal voltages provided by the CCE. Each motor incorporates a capacitive position sensor that provides position feedback to the CCE and allows the motors to be run under position control. This control loop provides high accuracy (±1%) control of the stroke amplitudes of the compressor pistons, which allows the cooler to achieve very high stability on the low-pressure side of the cooler and leads to excellent cold tip temperature stability (< 30 mK peak-to-peak). The CPA is mounted on shear force washers; these piezo-electric sensors provide a measurement of the forces exported in the axis of the CPA motors and allow the CCE to cancel these vibrations by modifying the drive waveforms in a feed-forward correction loop.
In addition to the items above, the CPA also incorporates thermistors which provide temperatures of both external and internal components of the mechanisms, along with the temperature reference point measurement.

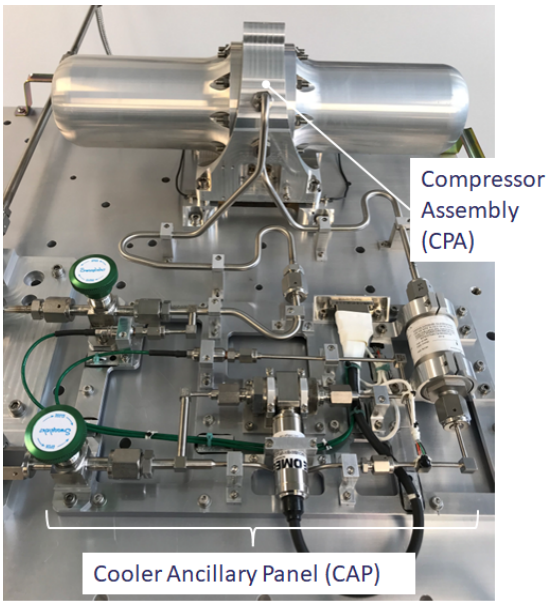

Figure 25: The Technology Demonstration Cooler CPA and CAP.

6.3 Cryocooler Auxiliary Panel (CAP)

The CAP incorporates the following electrical elements: a flow meter, high and low absolute pressure sensors, and thermometry. The flow meter works on the principle of differential pressure measurement: a high-resolution differential pressure sensor monitors the pressure drop through an orifice in the high-pressure flow line; this signal is combined with a temperature measurement at the orifice and the resulting values are used by the CCE to calculate the flow according to the orifice flow equation. The orifice flow coefficient is set during sensor calibration and can be entered into the CCE via telecommand. The absolute pressure sensors are tailored to the operating range of the cooler (~3–20 bar) and are calibrated during testing, with the calibration coefficients again being adjustable by telecommand. Thermometry is provided by nominal and redundant thermistors located at the flow meter orifice and the temperature reference point.

6.4 Cold tip heat exchanger (CHX)

The CHX contains all the cryogenic components of the cooler and runs from the Payload Interface Panel to the Telescope Optical Bench, where it interfaces with the AIRS detectors through a flexible thermal link. The CHX is instrumented with thermometry and – at the cold tip – heaters. The thermometry provides nominal and redundant temperature measurement at each thermal interface. To enable the CCE read-out chain to achieve the required accuracy and resolution over the full temperature range, different sensor types are used at different temperatures: platinum resistance thermometers (PT1000s) are used at the warmer stages (CWF, VG1 and VG2) and Cernox™ sensors are used at the colder stages (VG3 and the cold tip). At the cold tip, there are nominal and redundant instances of two types of heaters. The first is an orifice heater, which is used in the unlikely event that the fill gas contains impurities at a sufficient level to freeze out at the JT orifice and block it. The second is a boil-off heater that may be required if the liquid neon created by the JT expansion is not fully contained by the cold tip reservoir in zero-gravity; should this occur, the boil-off heaters are placed on the cold tip return line to prevent liquid from entering the heat exchanger, which could lead to uncontrolled boiling and temperature fluctuations at the cold tip.

7. HARNESS DEFINITION AND STATUS

The Ariel harness is a complex system, composed of many different subsystems and providers in terms of responsibility, procurement (Prime Contractors and Subcontractors), technical specification, AIT/AIV and routing.
As a first description, it can be split in two parts: the isothermal warm harness residing into the SVM, in charge of ESA and ADS (as Satellite Prime) and the cold harness residing in the PLM section and composed of a thermal gradient section, in charge of CSA (Canadian Space Agency) and ABB Canada (as CSA Prime Contractor) and an isothermal section in charge of AMC and CSA for what concern the AIRS isothermal section.
The PLM harness system responsibilities are illustrated in Table 2, where CSA has been recently selected as provider also for the FGS chryoharness (CH).
In addition, the harness complexity further increases when different procurements for different models (EM, EQM, PFM) and on-ground testing purposes (Test Harness) need to be taken into account.

Activity	AIRS Harness	FGS Harness	M2M Harness	TA Thermal Harness	DEC/SUR Harness	ACS Harness	VGR Sensors Harness
Common Requirement Definition	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team
Requirement Responsible	CEA	CBK	IEEC/Sener w/ TA Team	TA Team	RAL Space	RAL Tech	BGC
Routing Definition	Sys Team	Sys Team	Sys Team (BIP/VGR) TA Team (TA)	Sys Team (BIP/VGR) TA Team (TA)	Sys Team (BIP/VGR) DEC: TA Team (TA) SUR: Sys Team	Sys Team (BIP/VGR) TA Team (TA)	BGC (VGR) Sys Team (BIP)
Preliminary Definition	Canadian CH Provider	FGS CH Provider	Sener	Canadian CH Provider	Canadian CH Provider	RAL Tech	BGC
Approval of Preliminary Definition	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team
Detailed Definition	Canadian CH Provider	FGS CH Provider	Sener	Canadian CH Provider	Canadian CH Provider	RAL Tech	BGC
Approval before Procurement	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team
Procurement	Canadian CH Provider	FGS CH Provider	Sener	Canadian CH Provider	Canadian CH Provider	RAL Tech	BGC
Harness Level Test & Verification	Canadian CH Provider	FGS CH Provider	Sener	Canadian CH Provider	Canadian CH Provider	RAL Tech	BGC
Integration at Instrument/Subsystem	N/A	N/A	TA Team	TA Team	TA Team (for TOB sections)	RAL Tech	BGC
Integration at PLM	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team	Sys Team & RAL Tech	Sys Team

Table 2. PLM Harness System responsibility (CH stays here for CryoHarness). DEC/SUR harness refers to the Decontamination and Survival lines (both including heaters and thermistors) PLM section.

7.1 SVM harness (isothermal)

The PL SVM-located harness, including DEC and SUR warm sections, is the warm harness interconnecting the PL warm units and connecting them with the S/C avionic systems located into the SVM. In addition, it also includes the warm sections connecting the PL warm units to the Payload IF Panel (PIP) located on top SVM and acting as mechanical, thermal and electrical IF between the satellite platform and the PLM. Here are located 4 Interface Connectors Panels (ICP) as mechanical and electrical IF hosting the needed clearances for SVM to PLM harness connectors mating and screwing. DEC and SUR lines are powered and controlled by the platform avionic systems.

7.2 PLM harness (cryo, thermal gradient and isothermal)

From the PIP ICPs, the PLM thermal gradient harness (including cold DEC and SUR section) departs to the PLM through the Vgrooves, reaching then the PLM isothermal part. In order to avoid heat conduction from the SVM to the cryogenic PLM, the thermal gradient cryoharness is provided with customized heat-sinking IF and thermal straps to the Vgrooves passive radiant coolers. As well as being a thermal IF, the heat-sinking IF are in addition electrical IF, connecting the cryoharness bundle overshields to the PL and S/C chassis (as spacecraft ground reference) in order to

limit as much as possible ground and common mode currents loops and minimizing the harness transimpedance for PL performance optimization.

8. CONCLUSIONS

This paper has provided an overview of the Ariel Payload electrical and electronic architecture [20], on-board instruments and subsystems, harness included, their current implementation status and the way forward to the next Payload milestone: the PL CDR (pCDR), whose Kick Off Meeting is expected by end of 2025.

Further details on the overall Payload design and current status can be found in [21].

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