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A CHARGE SENSITIVE PREAMPLIFIER FOR SURFACE BARRIER DETECTORS

by

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1. INTRODUCTION

It is expected that a large number of solid state surface barrier detectors will be used in experiments at the Nuclear Structure Facility (NSF) at the Daresbury Laboratory. A high performance general purpose preamplifier for use with such detectors has been developed and this note describes the circuit and design details.

The preamplifier has been developed and engineered jointly by the Laboratory and Cooknell Electronics.

2. DESIGN CONSIDERATIONS

The specification of the preamplifier (Appendix A) has been drawn up with a view to providing a general purpose instrument. The range of detectors that will be connected to the preamplifier requires it to be capable of operating with a wide range of detector capacitances, from zero to 1000 pF.

Since the preamplifier may be located remote from the main shaping amplifier the output requires to be sending end terminated and capable of providing a high signal output voltage.

The noise characteristics have been specified to provide optimum performance with large capacitance detectors.

For operation in high resolution analogue channels, the preamplifier should have a better linearity and temperature coefficient than high grade spectroscopy amplifiers.

The preamplifier must be capable of operating in a severe electrical interference environment, particular attention being paid to the enclosure and electrical connectors.

3. PRINCIPLE OF OPERATION

A simplified schematic diagram of the preamplifier is shown in fig.1.

A cascode connected low noise input FET, TR_1 and a common base transistor TR_2 feed current to a wideband current gain stage, formed by transistors TR_3 and TR_4. Following that, a common base stage TR_5 develops an output voltage across an active load TR_6. Transistors TR_7 to TR_{10} form a unity gain buffer which drives the output through a cable matching resistor R_2. The feedback capacitor C_1 determines the charge sensitivity of the preamplifier and the parallel combination of C_1 and R_1 determines its decay time constant T_1 given by

$$T = C_1 \times R_1 \quad (1)$$

The open-loop gain A_{vo} of the circuit is determined by the transconductance g_{m1} of the input FET, the gain of the current gain stage and the effective load impedance Z_L at the collector of TR_5 as shown below

$$A_{vo} = g_{m1} A_i Z_L \quad (2)$$

where Ai = gain of the current amplifying stage (TR_3 and TR_4)

4. CIRCUIT DESCRIPTION

The full circuit diagram of the preamplifier is shown in fig.2. It includes an "EHT" connection which supplies bias to a surface barrier detector connected to the input. This supply is filtered by a two stage low pass network formed by R_1, R_4, R_5 and C_4, C_5. Also shown is a terminated "Test" input which feeds the main input through a capacitor C_3 adjusted to the same value as the feedback feedback capacitor C_2. A "Timing" output is obtained by differentiating the "Energy" output in C_{23} and R_{37}.

Transistor TR_{11}, with a heavily decoupled base, filters the power supply between the power output stages and the input transistors. The circuit was designed for optimum noise performance and a full noise analysis is given in Appendix C.

Although provision for input protection is made on the printed circuit board, this is not shown, since it is not possible to fully protect

the input FET without increasing the input noise. Diode D_3 protects the second transistor in the event of an EHT breakdown, and so limit any damage to TR_1.

Potentiometer RV_1 enables the quiescent "Energy" output to be set to 0 V.

To ensure stability several gain control networks are used. These are fully described in Appendix B. The d.c. power to the preamplifier is filtered using series ferrite inductors L_2, L_3 and feed through capacitors C_{24}, C_{25}. The sensitive circuits are electromagnetically shielded from the filter circuits of the d.c. power and EHT bias supplies. To ensure good screening, the preamplifier is housed in a 130 mm × 105 mm × 30 mm copper plated steel case, which is further tin plated for aesthetic reasons. All connectors are flange mounted to ensure good contact with the case.

Figure 3 shows the complete preamplifier with its lid removed.

5. TEST RESULTS

5.1 Sensitivity

The preamplifier was found to respond like a true charge sensitive amplifier with a sensitivity given by

$$S_E = \frac{q_e}{\varepsilon C_F} \frac{V}{eV} \qquad (3)$$

where q_e - charge of an electron

ε - energy required to create an electron ion pair (3.6 eV for Si)

C_F - value of feedback capacitor.

In the preamplifier the feedback capacitor C_2 (fig.2) is set to nominally 2 pF, giving a sensitivity of 22.4 mV/MeV.

The "Test" capacitor C_3 is also set to 2 pF, thus givhe circuit a gain of unity for "Test" signals.

5.2 Noise

Measurement of equivalent input noise was carried out using an Ortec 450 research amplifier set to a range of equal integrating and differentiating time constants.

The results plotted in fig.4 show for 1 μs shaping constants a noise of 3 keV for zero detector capacitance and of 23 keV for a 1000 pF detector. The latter is equivalent to a "noise slope" of 23 eV/pF, which is higher than predicted by eqn.(71) (Appendix C). Part of the difference is accounted for by the rather poor frequency response of the Ortec 450 amplifier, which for 1 μs shaping has a measured high frequency rolloff of approximately 60 db/decade, corresponding to three effective integrators.

It can be shown that a shaping amplifier with three integrators would give a noise slope 2.3 eV/pF greater than calculated in eqn.(70) for four integrators. The remaining difference is mainly due to the simplified noise model of the input FET and the resulting expression for series noise voltage in eqn.(42).

The noise measured with no detector capacitance is less than predicted by eqn.(65). 0.3 keV of the difference can be accounted for by the three instead of the expected four integrator response of the Ortec 450 amplifier

5.3 Rise Time

Rise time was measured for a 1 V output pulse into a 50 Ω load. The results are tabulated in fig.5 and show good agreement with calculations in Appendix C.

5.4 Effective Dynamic Input Capacitance

Connecting a 1000 pF capacitor across the input of the preamplifier results in a 3.5% drop in peak output for 1, 2 and 5 μs shaping constants, indicating a dynamic input capacitance of approximately 30000 pF.

5.5 Temperature Coefficient

The output level drift and temperature coefficient of gain were measured over a +10°C to +50°C temperature range, using a 50 Ω load.

The d.c. level drift was less than 1 mV over the full temperature range and the average temperature coefficient of gain was -150 ppm/°C.

5.6 EHT Breakdown

The EHT breakdown was measured by feeding the preamplifier output through a 1 μs shaping spectroscopy amplifier into a discriminator-rate-meter. With the discriminator set to 6 db above electronic noise level, the EHT bias to the preamplifier was increased from 0 V to 1.2 kV resulting in a breakdown pulse rate of 0.5 counts/s over a period of 100 seconds.

5.7 Output Amplitude

Linear response was obtained for output pulses up to ± 5 V into a 50 Ω load or ± 11 V into a 1 kΩ load.

5.8 Linearity

Integral linearity was measured with a 50 Ω load. Measurements at 1 V increments from 1 V to 5 V with 1 μs shaping showed the nonlinearity to be less than 0.03% of full (5 V) scale.

6. CONCLUSIONS

Two prototype preamplifiers have been constructed and are currently undergoing evaluation tests with charged particle detectors.

The measured "noise slope" meets the design specification given in Appendix A. It should be possible to reduce it by using selected input FET's.

The measured equivalent input noise with zero detector capacitance is higher than the design objective, but that is largely due to a requirement for a relatively low value of EHT bias resistor, 10 MΩ. By increasing the values of the bias resistor and of the 22 MΩ feedback resistor, it is possible to reduce that noise.

The preamplifier shows a 3.5 times greater sensitivity of output to detector capacitance than aimed for in the target specification. To meet that specification would require a 10 db increase in the preamplifier's open-loop gain. However it is felt that the above short-coming will be insignificant under experimental conditions.

The -150 ppm/°C temperature coefficient of gain is due mainly to the temperature coefficient of the cable matching resistors $R3_8$ and R_{39} (fig.2). In production units these will be changed and it is expected that the overall temperature coefficient will be halved.

7. ACKNOWLEDGEMENTS

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APPENDIX A

PROVISIONAL SPECIFICATION OF A GENERAL PURPOSE CHARGE SENSITIVE PREAMPLIFIER

Sensitivity:	20 mV/MeV
Input pulse polarity:	+ve or -ve
Output polarity:	inverse of input
Noise*:	< 2 keV FWHM
Noise slope*:	< 25 eV FWHM/pF
Rise time:	< 50 ns with zero detector capacitance
Decay time:	50 μs
Timing output rise time:	< 50 ns with zero detector capacitance
Sensitivity of output to detector capacitance:	$< 10^{-5}\ \frac{1}{pF}$
Maximum output voltage from 50 Ω series output:	± 5 V into 50 Ω
Integral nonlinearity:	< 0.1%
Connectors:	input, test, output, timing - BNC
	EHT bias - SHV
	power - 2 pole BNC
Power supply	± 12 V
Package:	steel, 130 mm × 70 mm × 58 mm

*Si equivalent noise measured with Ortec 450 research amplifier at 1 μs equal shaping constants.

APPENDIX B

GAIN AND STABILITY CALCULATIONS

The circuit has effectively seven active devices in the forward signal path. Even though the majority of these have cutoff frequencies in excess of 1 GHz, the total propagation delay was measured as approximately 5 ns. This would contribute 90 degrees of phase shift at 50 MHz, therefore to ensure stability, the unity loop gain crossover frequency should be less than 50 MHz.

The low frequency open loop voltage gain of the circuit is given in eqn.(2). The low frequency current gain of the current gain stage shown in fig.2 is given by

$$A_i = \frac{R_{13}}{R_{21}} + 1 = 55 \qquad (4)$$

The effective load impedance Z_L at the collector of TR_5 in fig.1 is approximately 20 kΩ with the preamplifier output terminated in 1 kΩ, but reduces to approximately 10 kΩ when terminated in 50 Ω. To reduce the effect of variation in Z_L on the open loop response, a fixed 22 kΩ resistor R_{19} is added between the collector of TR_5 and earth, thus reducing Z_L to approximately 10 kΩ and giving an open loop gain of

$$A_{vo} = q_{im1} A_i Z_L = 2 \times 10^4 = 86 \text{ db} \qquad (5)$$

for a q_{im1} of 35 mA/V.

The dominant lag is determined by stray capacitance at the collector of TR_5. The input capacitance of the output buffer is negligible due to the bootstrapping of the buffer input transistors TR_7 and TR_8 and so the total stray capacitance is relatively small and estimated to be approximately 5 pF. This gives rise to a break frequency of

$$f_o = \frac{1}{2\pi C_s Z_L} = 3 \text{ MHz} \qquad (6)$$

where C_s is the stray capacitance at the collector of TR_5.

To control the gain bandwidth produced, a 5.6 pF capacitor C_{15} in series with a 560 Ω resistor R_{20} is connected between the collector of TR_5 and earth, so reducing the break frequency to

$$f_o = \frac{1}{2\pi(C_5 + 5.6\ pF)Z_L} = 1.5\ MHz \qquad (7)$$

Frequency stabilisation is achieved by controlling the open loop gain as well as the feedback fraction. Two possible schemes of controlling the forward gain are shown in fig.2; one is based on two transitional lags determined by R_{25} = 1 kΩ, C_{25} = 100 pF and R_{26} = 330 Ω, C_{26} = 56 pF respectively, and a simpler one using a single transitional lag determined by R_{25} = 180 Ω, C_{25} = 330 pF.

To determine the loop bandwidth and stability of the amplifier, it is convenient to consider the forward open loop voltage gain from the gate of the input FET to the output of transistors TR_9, TR_{10} and the feedback path between that output and the input of the FET.

The forward open loop gain characteristic of the amplifier with a single transitional lag compensation of the TR_3, TR_4 doublet is shown in fig.5. The two corner frequencies associated with the above compensation are given by

$$f_1 = \frac{1}{2\pi\ C_{25} \times R_{13}} = 270\ KHz \qquad (8)$$

$$f_2 = \frac{1}{2\pi\ C_{25}\ R_{25}} = 2.7\ MHz \qquad (9)$$

The third break frequency is given by eqn.(7)

The feedback fraction is given by

$$\beta = \frac{C_2}{C_T + C_2} \qquad (10)$$

where C_2 - feedback capacitor shown in fig.2.

C_T - total input capacitance of the preamplifier.

The total input capacitance is the sum of the detector capacitance C_D and the open loop input capacitance C_i of the preamplifier.

$$C_T = C_D + C_i = C_D + C_{gs} + (g_{m1} Z_{L1} + 1)C_{gd} \qquad (11)$$

where C_{gs} - gate to source capacitance of the input FET

C_{gd} - gate to drain capacitance of the input FET

g_{m1} - transconductance of the input FET

Z_{L1} - drain load of the input FET

The third term in eqn.(11) represents the Miller capacitance of the FET.

In the circuit $C_2 \ll C_T$ and eqn.(11) simplifies to

$$\beta = \frac{C_2}{C_T} = \frac{C_2}{C_D + C_{gs} + (g_{m1} Z_{L1} + 1)C_{gd}} \qquad (12)$$

An L-R network inserted between the drain of the input FET and the emitter of TR_2 determines Z_{L1} and so controls the feedback fraction.

With zero detector capacitance eqn.(12) simplifies to

$$\beta_L = \frac{C_2}{C_{gs} + C_{gd}} \qquad (14)$$

and for high frequencies where the reactance of the 50 μH inductor exceeds 470 Ω, is given by

$$\beta_H = \frac{C_2}{C_{gs} + g_{m1} Z_{L1} C_{gd}} \qquad (15)$$

At high frequencies the drain load Z_{L1} is the parallel combination of R_6 and R_7

$$Z_{L1} = \frac{1200 + 470}{1200 + 470} = 340\ \Omega \qquad (16)$$

For C_{gs} = 30 pF and C_{gd} = 10 pF the feedback fraction for zero detector capacitance is

$$\beta_L = \frac{2}{40} \qquad (17)$$

for low frequencies, and

$$\beta_H = \frac{2}{150} = 0.133 = -37 \text{ db} \quad (18)$$

for high frequencies.

With a 1000 pF detector connected to the input of the preamplifier, eqn.(12) can be written as

$$\beta = \frac{C_2}{C_D} = \frac{2}{1000} = 0.002 = -54 \text{ db} \quad (19)$$

The closed loop gain is given by

$$A_{CL} = \frac{1}{\beta} \quad (20)$$

Figure 6 shows the open loop gain characteristics for the preamplifier with zero detector capacitance and with a 1000 pF detector connected. It shows closed loop bandwidths of 40 mHz and 6 MHz respectively, which would result in minimum pulse rise times of 9 ns and 60 ns.

Using two transitional lags in the current gain stage gives more loop gain at high frequencies but results in more overshoot in the pulse response with large capacitance detectors, due to reduced phase margin in the loop. The dotted line in fig.6 shows the open loop gain characteristic with such compensation. For zero detector capacitance the closed loop bandwidth is unaltered, but increases from 6 MHz to 9.5 MHz for a 1000 pF detector resulting in a corresponding decrease in minimum rise time from 60 ns to 37 ns.

A 10 pF capacitor C_{12} provides a low impedance load for transistor TR_4 at high frequencies (greater than the bandwidth of the complete preamplifier), thus aiding the stability of the current gain stage.

APPENDIX C

NOISE PERFORMANCE CALCULATIONS

The effect of noise in an amplifier can be analysed by representing all noise sources by an equivalent series noise source v_n and an equivalent parallel noise current i_n as shown in fig.7.

The effect of the equivalent parallel noise current can be analysed by considering a charge sensitive preamplifier followed by a shaping amplifier with equal integrating and differentiating time constants as shown in fig.8.

In practical circuits the equivalent preamplifier input capacitance $C_i \gg C_D$ and so all the noise current can be assumed to flow into the preamplifier.

The mean square output noise voltage due to i_n is given by

$$\overline{v_{no}^2} = \frac{1}{2\pi} \overline{i_n^2} \int |H(j\omega)|^2 \, d\omega \quad (21)$$

which for a white noise noise source can be written as

$$\overline{v_{no}^2} = \frac{\overline{i_n^2}}{2\pi} \int_0^\infty |H(j\omega)|^2 \, d\omega \quad (22)$$

where $H(j\omega)$ - transfer function from the input of the preamplifier to the output of the shaping amplifier.

For the circuit in fig.8

$$H(j\omega) = \frac{1}{j\omega C_F} \times \frac{j\omega T}{(1 + j\omega T)^2} \quad (23)$$

where T is the value of the shaping constants

$$T = C_1 R_1 = C_2 R_2 \quad (24)$$

substituting from eqn.(23) into eqn.(22)

$$\overline{v_{no}^2} = \frac{\overline{i_n^2}}{2\pi} \int_0^\infty \frac{T^2 \, d\omega}{C_F^2 (1 + \omega^2 T^2)} = \frac{\overline{i_n^2}}{C_F^2} \times \frac{T}{8} \quad (25)$$

Giving an rms output voltage,

$$v_{no} = \frac{i_n}{C_F}\sqrt{\frac{T}{8}} \tag{28}$$

The output of circuit in fig.8 due to an input charge q_s is given by,

$$V_{so}(t) = \int^{-1} \frac{q_s}{C_F}\,\frac{T}{(1+ST)^2} = \frac{q_s}{C_F\,T}\,t\,e^{\frac{-t}{T}} \tag{27}$$

The peak of the above output occurs at t= T and is

$$V_{somax} = \frac{q_s}{C_F\,e} \tag{28}$$

From eqns.(26) and (28), the eqivalent rms noise charge q_{ni} due to noise current i_n is,

$$q_{ni} = i_n\,e\sqrt{\frac{T}{8}} \quad \text{rms} \tag{29}$$

This corresponds to an eqivalent FWHM energy noise in a detector of,

$$E_{ni} = \frac{2.35\,i_n\,e\,\varepsilon}{q_e}\sqrt{\frac{T}{8}} \tag{30}$$

where ε - energy required to produce an electron ion pair in the detector

q_e - charge of an electron = 1.6×10^{-19} C

For a silicon detector ε = 3.6 eV, giving,

$$E_n = 5.1\,i_n\sqrt{T} \times 10^{19} \text{ eV FWHM} \tag{31}$$

which for equal 1 μs shaping time constants is,

$$E_n = 5.1\,i_n \times 10^{13} \text{ keV FWHM} \tag{32}$$

The effect of the equivalent series noise voltage can be analysed by considering the circuit shown in fig.9, in which the mean square output noise voltage due to input noise v_n is given by

$$\overline{V_{no}^2} = \frac{1}{2\pi}\int_0^{\infty} \overline{V_n^2}\,|H(j\omega)|^2\,d\omega \tag{33}$$

where the transfer function is,

$$H(j\omega) = \frac{C_D}{C_F} \times \frac{j\omega\,T}{(1+j\omega\,T)^2} \tag{34}$$

For a white noise source the mean square output noise is,

$$\overline{V_{no}^2} = \frac{C_D^2\,\overline{V_n^2}}{2\pi\,C_F^2}\int_o^{\infty} \frac{\omega^2\,T^2}{1+\omega^2\,T^2}\,d\omega = \overline{V_n^2}\,\frac{C_D^2}{8T\,C_F^2} \tag{35}$$

Giving an rms output noise of,

$$v_{no} = v_n\,\frac{C_D}{C_F\sqrt{8T}} \tag{36}$$

From eqns.(28) and (36), the equivalent rms noise charge q_n, due to a noise voltage v_n is,

$$q_n = v_n\,\frac{C_D\,e}{\sqrt{8T}} \tag{37}$$

This corresponds to an equivalent FWHM energy noise in a detector of,

$$E_n = v_u\,\frac{2.35\,C_D\,e\,\varepsilon}{q_e\sqrt{8T}} \tag{38}$$

which for a silicon detector is,

$$E_n = 5.1\,v_n\,\frac{C_D}{\sqrt{T}} \times 10^{19} \text{ eV FWHM} \tag{39}$$

For equal 1 μs shaping time constants the above gives,

$$E_n = 5.1\,v_n\,C_D \times 10^{22} \text{ eV FWHM} \tag{40}$$

This can be expressed as an equivalent "noise slope"

$$E_{ns} = 5.1\,v_n \times 10^{10}\ \frac{\text{eV FWHM}}{\text{pF}} \tag{41}$$

The most significant noise sources associated with the circuit in fig.2 are shown in fig.10

The series noise voltage generated by the input FET is given by,

$$V_{n1} = \sqrt{\frac{4 \times 0.7\,k\,T_j}{g_{m1}}} \tag{42}$$

where k - Boltzman constant

T_j - FET channel temperature

For the J109 (siliconix) FET operating with a g_{m1} = 35 mA/V and dissipating approximately 80 mW, the channel temperature will be approximately 20°C above ambient, giving

$$V_{n1} = 0.6 \ \frac{nV}{\sqrt{Hz}} \tag{43}$$

The 1.2 kΩ drain load resistor contributes,

$$V_{n2} = \frac{1}{g_{m1}} \sqrt{\frac{4k\ T_a}{R_6}} = 0.1 \ \frac{nV}{\sqrt{Hz}} \tag{44}$$

where T_a - ambient temperature.

Similarly the 1.8 kΩ feedback resistor R_{13} in the current gain stage contributes,

$$v_{n3} = \frac{1}{g_{m1}} \sqrt{\frac{4k\ T_a}{R_{13}}} = 0.1 \ \frac{nV}{\sqrt{Hz}} \tag{45}$$

The noise due to base current short noise in TR_2 is given by,

$$v_{n4} = \frac{1}{g_{m1}} \sqrt{2q_e I_b} \tag{46}$$

where I_b - base current in TR_2.

For an estimated base current of 50 μA the equivalent input noise is,

$$v_{n4} = 0.1 \ \frac{nV}{\sqrt{Hz}} \tag{47}$$

The total series noise due to the above uncorrelated noise source is,

$$V_{nT} = \sqrt{v_{n1}^2 + v_{n2}^2 + v_{n3}^2 + v_{n4}^3} = 0.62 \ \frac{nV}{\sqrt{Hz}} \tag{48}$$

It is seen that the total series noise is mainly due to the input FET.

Substituting into eqn.(41) gives a "noise slope" of

$$E_{ns} = 32 \ \frac{eV}{pF} \ \text{FWHM} \tag{49}$$

At zero detector capacitance the noise due to the series noise generator will be determined by the preamplifier's open loop input capacitance which for the J109 is 40 pF, giving

$$E_n = 40 \times 32 = 1300 \text{ eV} = 1.3 \text{ keV FWHM} \tag{50}$$

The parallel noise due to the FET gate leakage current is given by,

$$i_{n1} = \sqrt{2q_e I_G} \tag{51}$$

which for an estimated gate current I_G = 0.2 nA is

$$i_{n1} = 4.1 \times 10^{-15} \ \frac{A}{\sqrt{Hz}} \tag{52}$$

The noise due to the 22 MΩ feedback resistor R_2 is,

$$i_{n2} = \frac{4k\ T_a}{R_2} = 2.7 \times 10^{-14} \ \frac{A}{\sqrt{Hz}} \tag{53}$$

Similarly the noise due to the 10 MΩ EHT bias resistor R_1 is,

$$i_{n3} = \frac{4k\ T_a}{R_1} = 4.1 \times 10^{-14} \ \frac{A}{\sqrt{Hz}} \tag{54}$$

The total equivalent parallel noise is

$$i_{nT} = \sqrt{i_{n1}^2 + i_{n2}^2 + i_{n3}^2} = 4.9 \times 0^{-14} \ \frac{A}{\sqrt{Hz}} \tag{55}$$

From eqn.(32) it is seen that the noise generated by i_{nT} is

$$E_n = 5.1 \times 4.9 \times 0^{-14} \times 10^{-13} = 2.5 \text{ keV FWHM} \tag{56}$$

Thus at zero input capacitance the expected noise will be the sum of components given in eqns.(50) and (56),

$$E_{nT} = \sqrt{2.5^2 + 1.3^2} = 2.8 \text{ keV FWHM} \tag{57}$$

while for a 1000 pF detector, the expected noise will be the sum of the components given in eqn.(56) and the product of "noise slope" and detector capacitance giving

$$E_{nT} = \sqrt{2.5^2 + 32^2} = 32 \text{ keV FWHM} \tag{58}$$

It can be seen that for large capacitance detectors the noise will be

mainly determined by the "noise slope".

The above results are a useful measure of the preamplifier's noise performance, however noise measurements were carried out using an Ortec 450 reseach amplifier, which provides shaping equivalent to a single differential and four integrators. The output of the test circuit, shown schematically in fig.11 due to an input signal charge q_s is,

$$V_{so}(t) = \mathcal{L}^{-1} \frac{q_s T}{C_F(1 + sT)^5} = \frac{q_s t^4}{24 C_F T^4} e^{-t/T} \quad (59)$$

Producing a peak output of,

$$V_{somax} = 0.2 \frac{q_s}{C_F} \quad (60)$$

The mean square output noise voltage due to i_n is given by,

$$\overline{V_{no}^2} = \frac{1}{2\pi} \int_0^\infty \frac{d\omega}{(1 + \omega^2 T^2)^5} = 0.07 \frac{\overline{i_n^2}\, T}{C_F^2} \quad (61)$$

which corresponds to an rms noise of,

$$V_{no} = 0.26 \frac{i_n}{C_F} \sqrt{T} \quad (62)$$

From eqns.(60) and (62), the FWHM energy noise in a detector is,

$$E_n = 3 \frac{i_n \epsilon}{q_e} \sqrt{T} \quad (63)$$

For T=1 μs for a silicon detector this gives a noise of,

$$E_n = 7\, i_n\, 10^{13} \text{ keV FWHM} \quad (64)$$

substituting from eqn.(55) gives

$$E_n = 3.4 \text{ keV FWHM} \quad (65)$$

The mean square output due to the series noise v_n is,

$$\overline{V_{no}^2} = \frac{C_D \overline{V_n^2}}{2\pi C_F^2} \int_0^\infty \frac{\omega^2 T^2}{(1 + \omega^2 T^2)^5} d\omega = 0.01 \frac{V_n^2 C_D^2}{T C_F^2} \quad (66)$$

which corresponds to an rms noise of,

$$V_{no} = 0.1 \frac{v_n C_D}{C_F \sqrt{T}} \quad (67)$$

From eqns.(60) and (67) the equivalent rms energy noise in a detector is,

$$E_n = \frac{v_n C_D \epsilon}{2 q_e \sqrt{T}} \quad (68)$$

which for T=1 μs in a silicon detector corresponds to a "noise slope" of,

$$e_{ns} = \frac{E_n}{C_D} = 2.6\, v_n \times 10^{10} \frac{eV}{pF} \text{ FWHM} \quad (69)$$

Substituting for v_n from eqn.(48) gives,

$$E_{ns} = 16 \frac{eV}{pF} \text{ FWHM} \quad (70)$$

With no detector capacitance the contribution due to the series noise generator v_n is given by,

$$E_n = E_{ns} \times C_i \quad (71)$$

where C_i - input capacitance of the FET resulting in a noise of 640 eV FWHM.

The above contribution is much smaller than that given in eqn.(65), which will therefore determine the noise for small capacitance detectors.

FIGURE CAPTIONS

Fig.1 Simplified schematic diagram of the preamplifier.

Fig.2 Full circuit diagram of the preamplifier.

Fig.3 Photograph of preamplifier with the lid removed.

Fig.4 Noise performance curves.

Fig.5 Measured rise times.

Fig.6 Bode gain diagram.

Fig.7 Charge sensitive amplifier with equivalent noise sources.

Fig.8 Preamplifier with parallel input noise.

Fig.9 Preamplifier with series input noise.

Fig.10 Preamplifier with most significant noise sources.

where v_{n1} - series noise due to FET channel noise

v_{n2} - series noise due to resistor R_6

v_{n3} - series noise due to resistor R_{13}

v_{n4} - series noise due to base current shot noise in TR_2

i_{n1} - parallel noise due to FET gate leakage current

i_{n2} - parallel noise due to feedback resistor R_2

i_{n3} - parallel noise due to EHT bias resistor R_1

Fig.11 Preamplifier with Ortec 450 research amplifier.

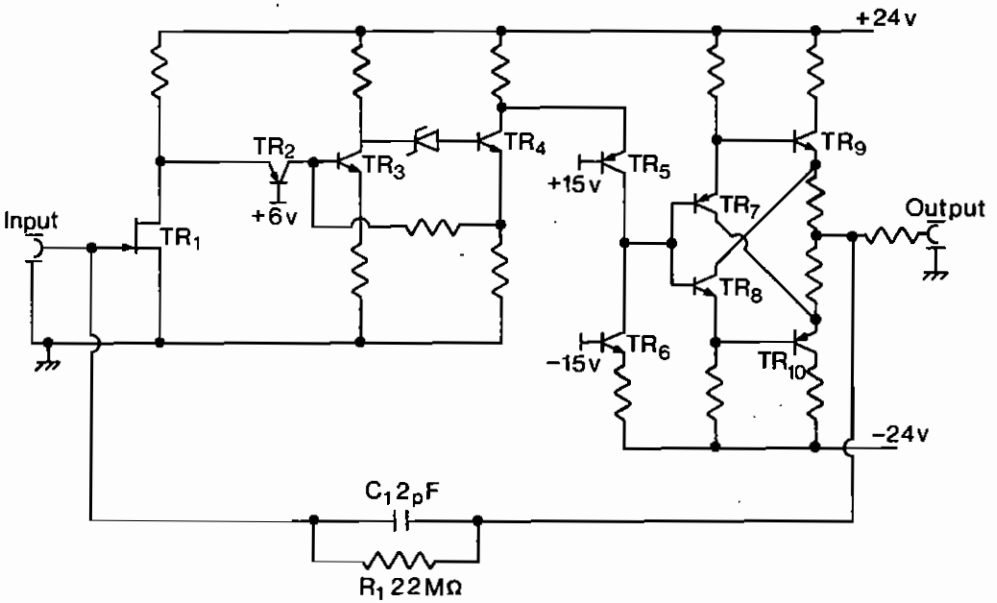


Fig.1

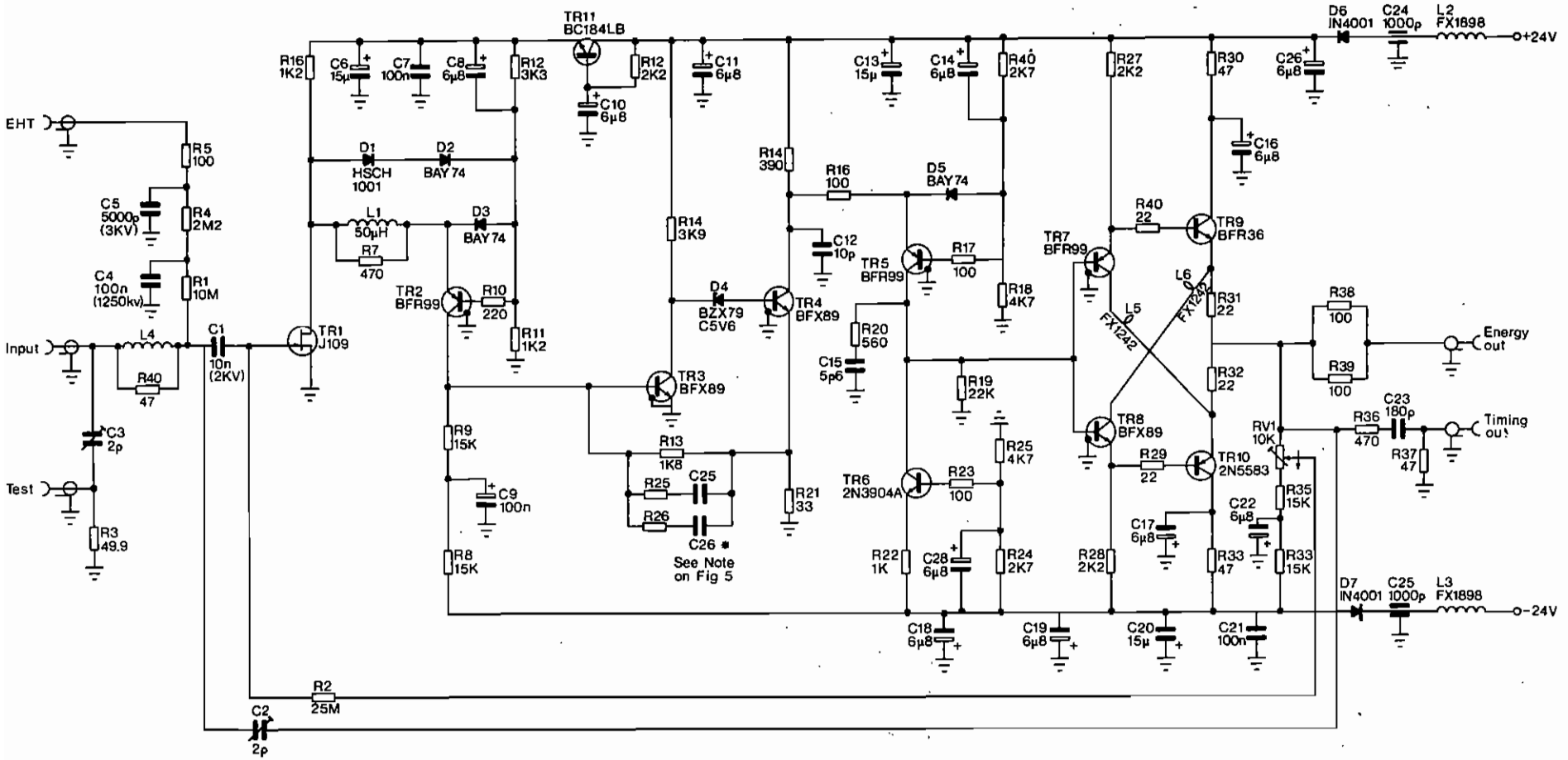

EHT
Input
Test
R5 100
R4 2M2
R1 10M
C5 5000p (3KV)
C4 100n (1250kv)
L4
R40 47
C1 10n (2KV)
C3 2p
R3 49.9
TR1 J109
R2 25M
C2 2p
R16 1K2
C6 15µ
C7 100n
C8 6µ8
R12 3K3
TR11 BC184LB
R12 2K2
C10 6µ8
C11 6µ8
D1 HSCH 1001
D2 BAY74
L1 50µH
R7 470
D3 BAY74
TR2 BFR99
R10 220
R11 1K2
R9 15K
C9 100n
R8 15K
R14 3K9
TR3 BFX89
R13 1K8
R25
C25
R26
C26 *
See Note on Fig 5
R14 390
R16 100
D5 BAY74
C12 10p
D4 BZX79 C5V6
TR4 BFX89
R21 33
C13 15µ
C14 6µ8
R40 2K7
TR5 BFR99
R17 100
R18 4K7
R20 560
C15 5p6
R19 22K
TR6 2N3904A
R23 100
R25 4K7
R22 1K
C28 6µ8
R24 2K7
C18 6µ8
C19 6µ8
C20 15µ
C21 100n
R27 2K2
TR7 BFR99
R40 22
TR8 BFX89
R29 22
R28 2K2
L5 FX1242
L6 FX1242
TR9 BFR36
R30 47
C26 6µ8
C16 6µ8
R31 22
R32 22
TR10 2N5583
R33 47
C17 6µ8
C22 6µ8
R35 15K
R33 15K
D6 IN4001
C24 1000p
L2 FX1898
+24V
D7 IN4001
C25 1000p
L3 FX1898
-24V
R38 100
R39 100
Energy out
RV1 10K
R36 470
C23 180p
R37 47
Timing out

Fig.2

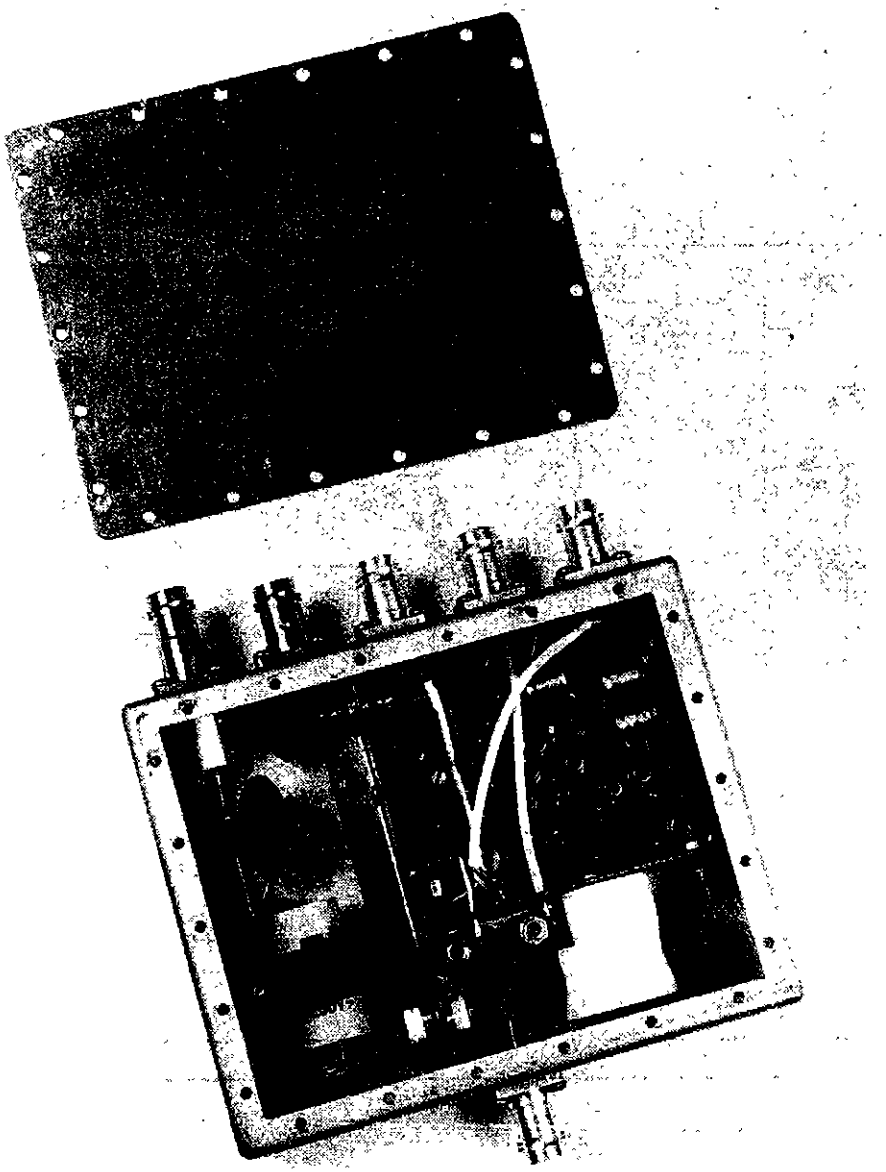


Fig.3

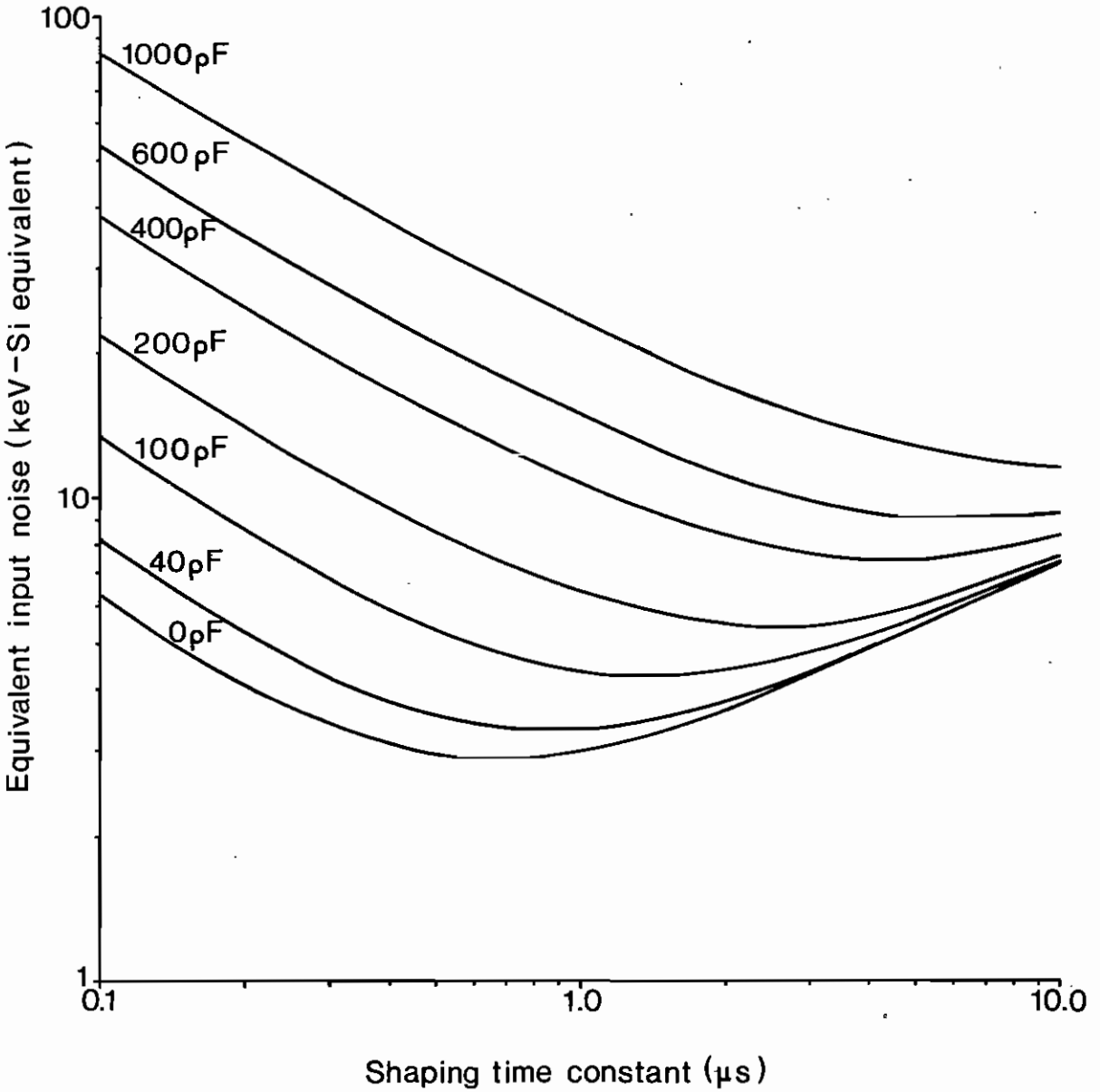

100
10
1
1000pF
600pF
400pF
200pF
100pF
40pF
0pF
0.1
1.0
10.0
Equivalent input noise (keV-Si equivalent)
Shaping time constant (μs)

Fig.4

	Risetime (10% - 90%)	
Compensation *	Detector capacitance 0 pF	1000 pF
Single lag	10 ns	70 ns
Double lag	10 ns	35 ns

* Two transitional lags R25 = 1kΩ, C25 = 100 pF
R26 = 330Ω, C26 = 56 pF

One transitional lag - omit R26 and C26
R25 = 180Ω, C25 = 330 pF

Fig. 5

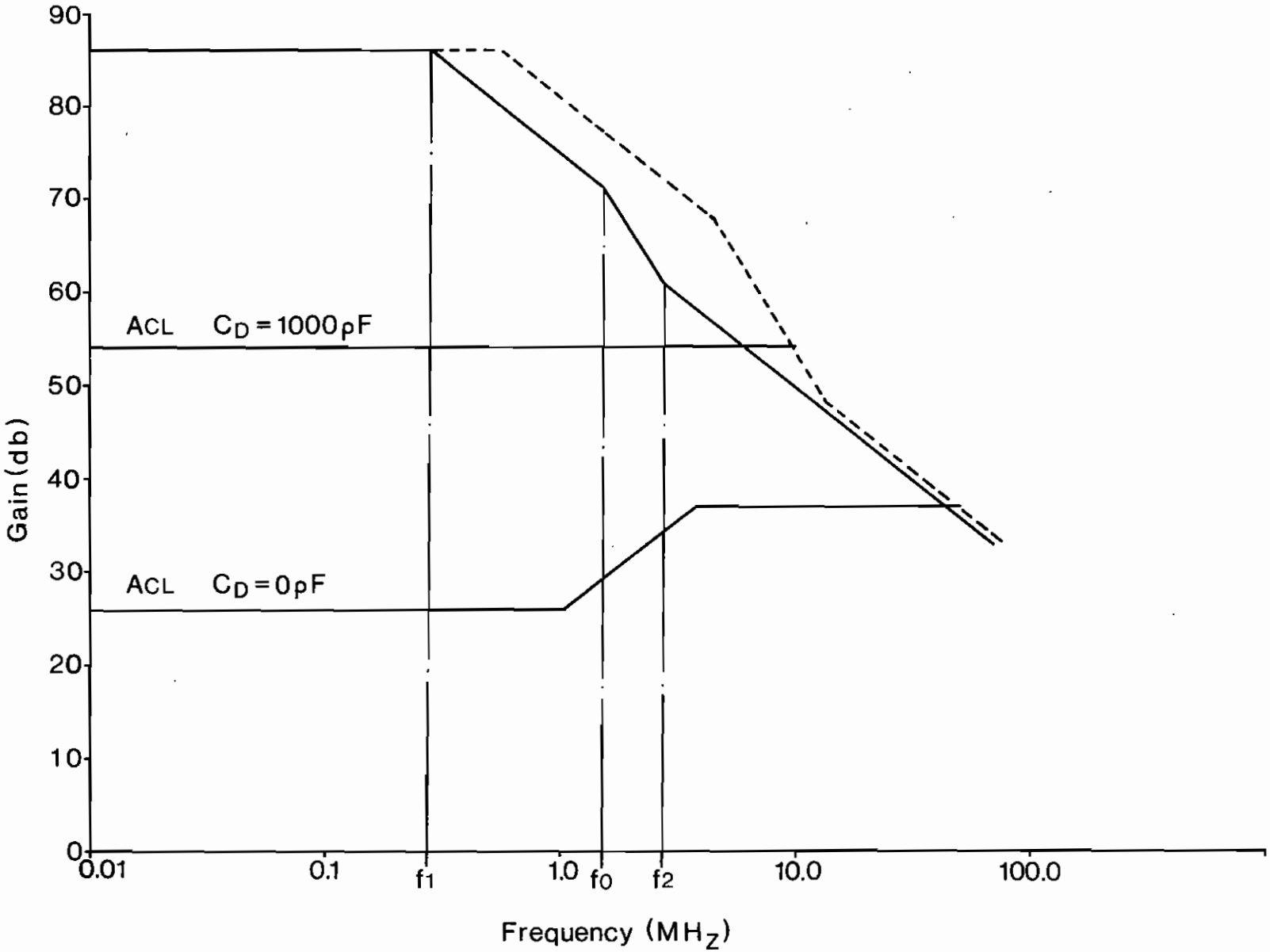

90
80
70
60
50
40
30
20
10
0
Gain (db)
ACL $C_D = 1000pF$
ACL $C_D = 0pF$
0.01
0.1
f_1
1.0
f_0
f_2
10.0
100.0
Frequency (MH_Z)

Fig.6

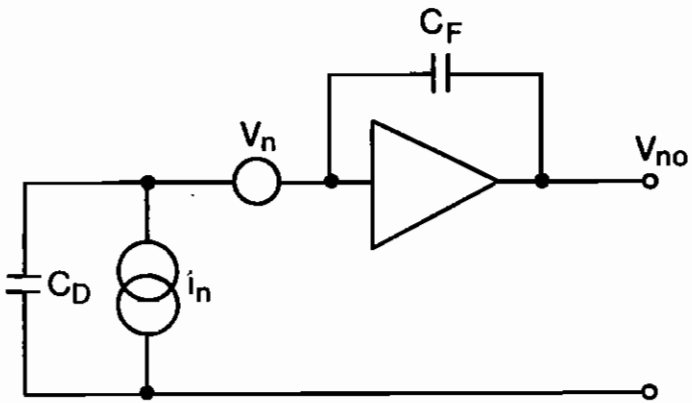


Fig.7

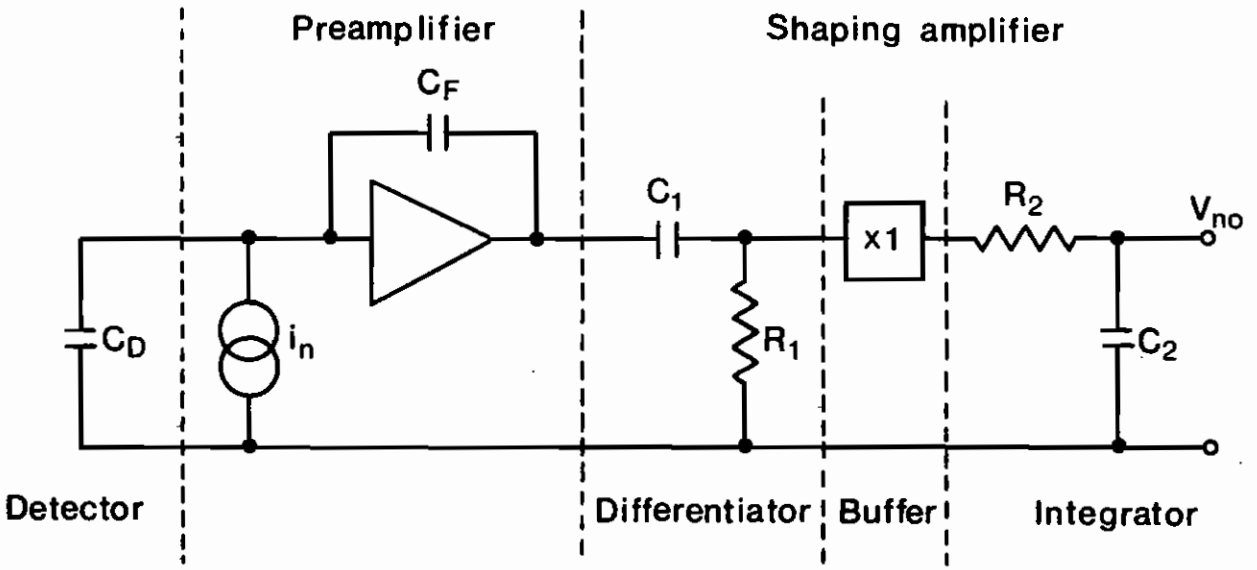

Preamplifier
Shaping amplifier
C_F
C_1
R_2
V_{no}
x1
C_D
i_n
R_1
C_2
Detector
Differentiator
Buffer
Integrator

Fig. 8

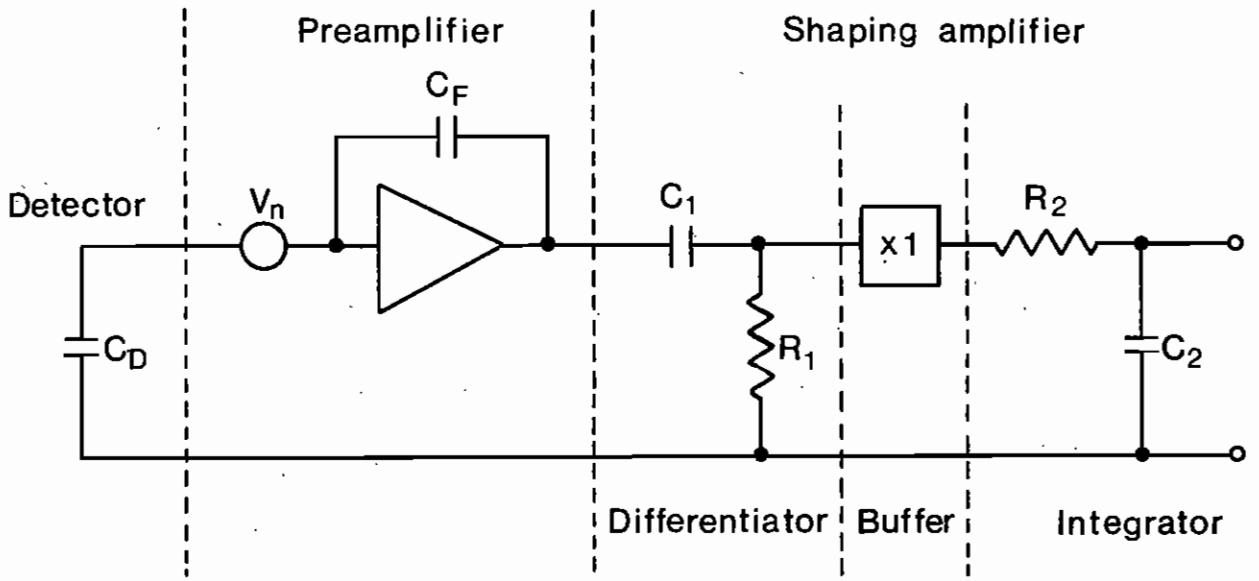

Preamplifier
Shaping amplifier
C_F
Detector
V_n
C_1
x1
R_2
C_D
R_1
C_2
Differentiator
Buffer
Integrator

Fig. 9

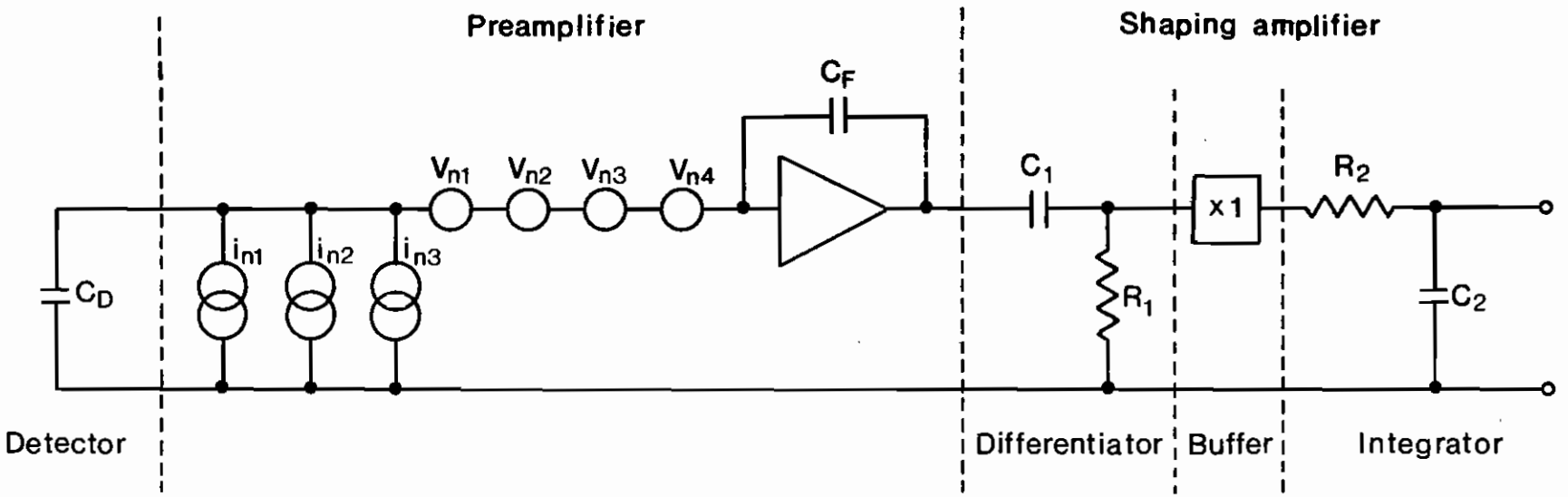
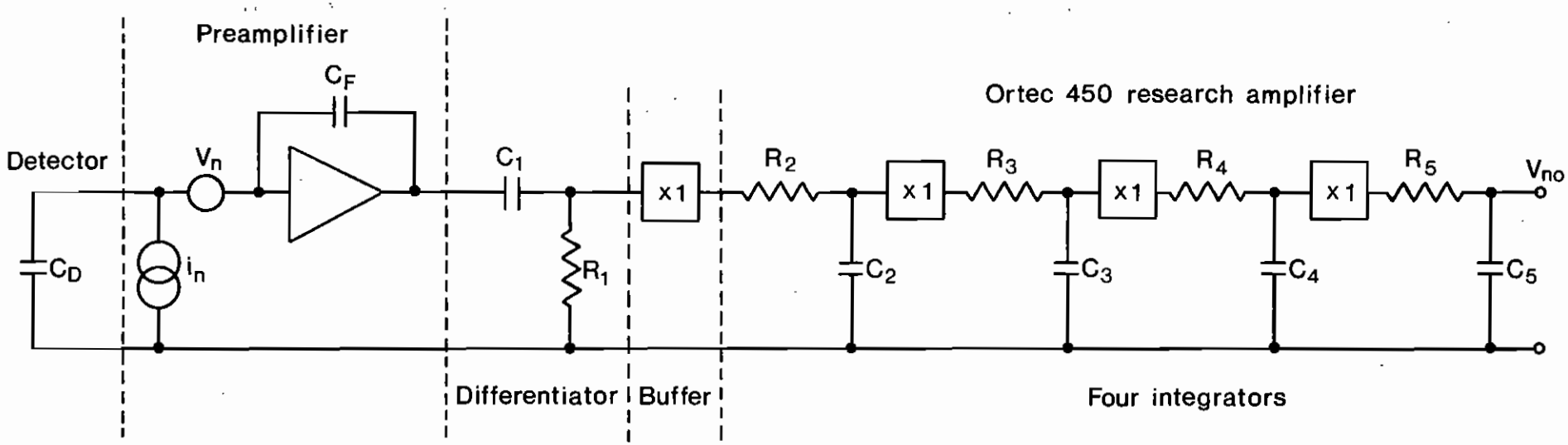

Preamplifier
Shaping amplifier
C_F
V_{n1}
V_{n2}
V_{n3}
V_{n4}
C_1
R_2
x1
i_{n1}
i_{n2}
i_{n3}
C_D
R_1
C_2
Detector
Differentiator
Buffer
Integrator

Fig.10



$$C_1R_1 = C_2R_2 = C_3R_3 = C_4R_4 = C_5R_5 = T$$

Fig. 11