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ORGANISATION OF COMMUNICATIONS TO LARGE CAPACITY MEMORY SYSTEMS VIA CAMAC: AUXILIARY CAMAC MEMORY BUS

by

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ABSTRACT

An auxiliary bussing system is described which permits transfers from a CAMAC control unit to external bulk semiconductor memory. It is capable of supporting data transfer rates in excess of 2 MHz.

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1. INTRODUCTION

The decrease in costs of semiconductor devices has made the use of large capacity memories an economical possibility in data collection and processing systems. In addition to decreasing costs there has also been an increase in their operating speed. Typical access times of Random Access Memories (RAM) ranges from 100 ns to 350 ns. The relatively high speed of these memories has meant that their performance could not be fully exploited if used in a CAMAC system communicating via the standard dataway[1], consequently consideration has been given to providing an auxiliary bussing system which augments the CAMAC dataway.

There are currently a number of proposals by various international organisations for suitable systems/bussing to accommodate the higher speed and more complex semiconductor devices which are now available. In the absence of any firm agreement as to international standards and the pressing need to provide a large capacity, high speed memory system[2] a bussing system has been specified and is incorporated in a memory system being developed by the Daresbury Laboratory.

2. BASIC FEATURES OF THE BUS

2.1 Concept

The bus is intended to allow communication between a "Control Unit" which meets the requirements of CAMAC [EUR 4100e] and a "dumb memory" which optionally can be contained in CAMAC modules or any other suitable mechanical format which provides the appropriate power supply. To provide a bus which has the ability to communicate with up to 16 million locations, each with a depth of up to 24 bits, would require an unwieldy number of lines. The bussing system described, uses a common time multiplexed address/data bus of 24 lines with additional lines for control. Multiplexing introduces a slight reduction in speed but gives a significant reduction in address/data lines and manufacturing costs.

2.2 Basic Features

The basic features may be summarised as follows:

(i) The bus provides a bi-directional time multiplexed address/data connection from an external memory to a CAMAC environment.

(ii) The bus provides addressing and data lines to a capacity of up to 24 bits.

(iii) Memory modules can be independent of mechanical format.

(iv) Timing arrangements are such as to permit transfers at $2\times10^6 s^{-1}$.

3. USE OF THE BUS LINES

Communication between a memory control unit and the memory is via a 40 way flat ribbon cable. The connector on the control unit (CAMAC) is on the rear panel. When CAMAC format is used for memory modules the bus lines link corresponding pins on all modules.

A typical bus operation involves at least two units, a controller and a memory module.

During a bus operation the controller generates a multiplexed command which consists of an address plus control signals, followed by data plus control signals. Address and data transactions are controlled by a two way handshake incorporated in the bus control lines.

3.1 Memory Bus Functions

The bus consists of:

24	Address/data lines
11	Control/status lines
5	Ov lines

AD01 - AD24 Address/data lines.
The lines provide a time multiplexed bi-directional communication path for address and data.

C0 C1 CLEAR Control lines from controller to memory describing the type of memory cycle to be performed.

C0	C_1	CLEAR	
0	0	0	Read
1	0	0	Write
0	1	0	Not used
1	1	0	Direct Memory Modify (DMM)
x	x	1	Clear.

O FLO ENB Bit set. From controller. Overflow enable sets a latch in the memory module. Permits contents of memory location to overflow during DMM cycle.
Bit not set. Restores the contents of the memory location to its original value on an overflow operation.

O FLO Overflow. From memory. Bit set indicates overflow has taken place. It is present if OFLO ENB has not been set.

PAR ERR Parity Error. From memory. Bit set by a detected parity error on a READ operation or a READ part of a DMM cycle.

INIT Initialise. From controller. Initialises the memory and delatches all control states. Duration > 1 μs.

ADSTR Address strobe. Generated by control module. The leading edge of this signal clocks address and control signals AD01 - AD024, C0, C_1, CLEAR, O FLO, ENB into the memory module.

ADOK Valid address. (From memory module). The addressed memory module responds if correctly addressed. The controller responds by removing ADSTR and AD01 - AD24. Removal of ADSTR removes ADOK.

DINC Generated by the control module at the start of the DATA part of a cycle. It strobes data into the memory module on a WRITE or DMM operation. It must appear > 25 ns after AD01 - AD24.

DOUTC Memory cycle complete.
On completion of the memory operation DOUTC is generated. On a READ cycle the leading edge of DOUTC clocks data into the control unit. DINC is cleared by DOUTC. DOUTC in

turn is cleared by the removal of DINC. The duration of DOUTC or greater than 50 ns is sufficient to permit transfer of data and must appear greater than 25 ns after ADO1 - ADO24.

4. TIMING OF BUS SIGNALS

The sequence of events during a bus operation is shown in figs.1, 2, 3 and 4 by means of simplified signal waveforms. As the bus operation is based on an interactive handshake absolute times are not shown except where minimum set up times are necessary.

Rise and fall times < 25 ns.

ADO1 - ADO24 are driven by the control unit except during the data part of a READ cycle.

Timing dispersion on the bus < 25 ns, i.e. data must be stable 25 ns before a strobe is initiated.

Leading edge of strobe DOUTC(READ),DINC(WRITE), is used to clock data.

Time out facilities should be included in the Controller if an ADOK response is not obtained within an appropriate period.

5. BUS SPECIFICATION

5.1 Mechanical Arrangement

40 way flat cable type 3M 3365 is terminated in insulation displacement connectors (IDC) type 3M 3417/xxxx which mate to connectors type 3M 3495/xxxx mounted on the modules. Maximum cable length is 0.5 m.

5.2 Electrical Connectors

5.2.1 Signal levels

TTL compatible, High = logic 0, 2.0 V to 3.0 V, Low = logic 1, 0 V to 0.8 V. All signal lines terminated at the control station end by a resistive network with an impedance of 100 Ω (fig.5).

5.2.2 Contact assignment

See table 1.

5.2.3 Loading Each station must not load any line of the bus by more than 200 mA at 3.4 V and 0.2 mA at 0.8 V.

Driving Each driver must have a sink capability of 64 mA.

6. CONCLUSIONS

A bussing system has been specified and incorporated into a large capacity memory readout system. It presents an economical and convenient method of interconnection using the limited available space on a CAMAC rear panel.

1. CAMAC Organisation of Multicrate Systems EUR 4600.

2. J.R. Helliwell, G. Hughes, M.M.Przybylski et al. A 2D MWPC area detector for use with synchrotron x-radiation at the Daresbury Laboratory for small angle diffraction and scattering. Daresbury Laboratory Report DL/SCI/P 269E (1981).

TABLE 1

Contact assignment for 40 way IDC connector

1	0V	2	AD01
3	AD02	4	AD03
5	AD04	6	AD05
7	AD06	8	AD07
9	AD08	10	0V
11	AD09	12	AD10
13	AD11	14	AD12
15	AD13	16	AD14
17	AD15	18	AD16
19	AD17	20	0V
21	AD18	22	AD19
23	AD20	24	AD21
25	AD22	26	AD23
27	AD24	28	0V
29	OFLO ENB	30	DINC
31	C1	32	PAR ERR
33	C0	34	ADSTR
35	INIT	36	0V
37	ADOK	38	DOUTC
39	ADOK	40	CLEAR

FIGURE CAPTIONS

Figure 1 Timing diagram READ operation.

Figure 2 Timing diagram WRITE operation.

Figure 3 Timing diagram CLEAR operation.

Figure 4 Timing diagram DIRECT MEMORY MODIFY operation.

Figure 5 Termination of each signal line.

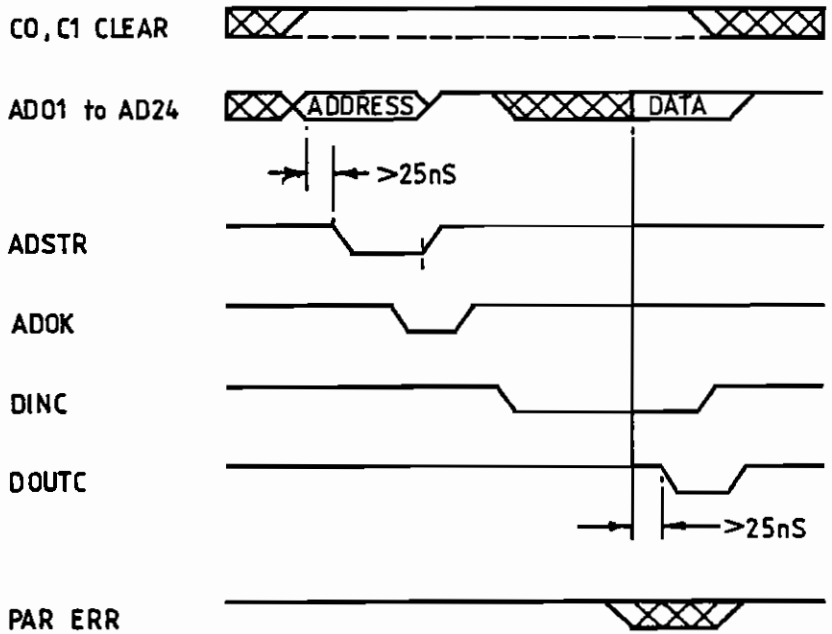

FIG 1

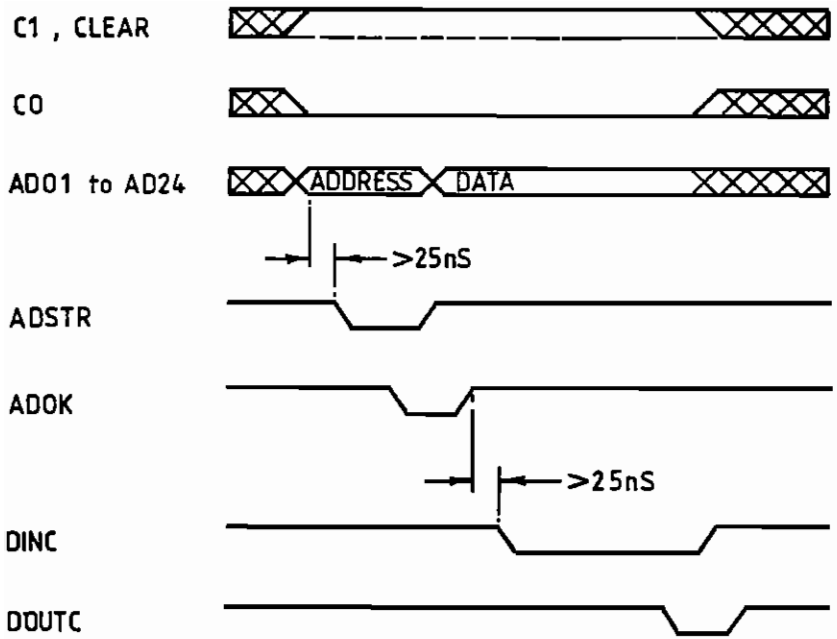
C1 , CLEAR
CO
AD01 to AD24
ADDRESS
DATA
>25nS
ADSTR
ADOK
>25nS
DINC
DOUTC

FIG 2

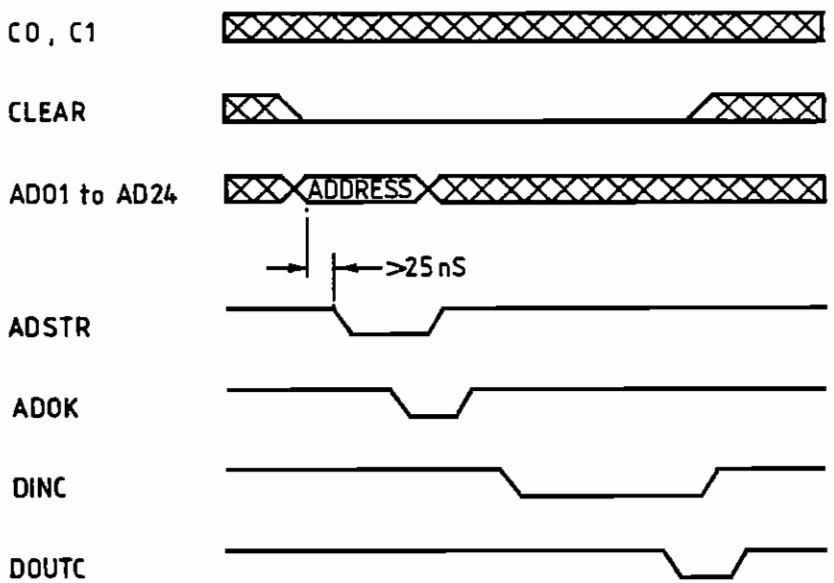
CO , C1
CLEAR
AD01 to AD24
ADDRESS
>25nS
ADSTR
ADOK
DINC
DOUTC

FIG 3

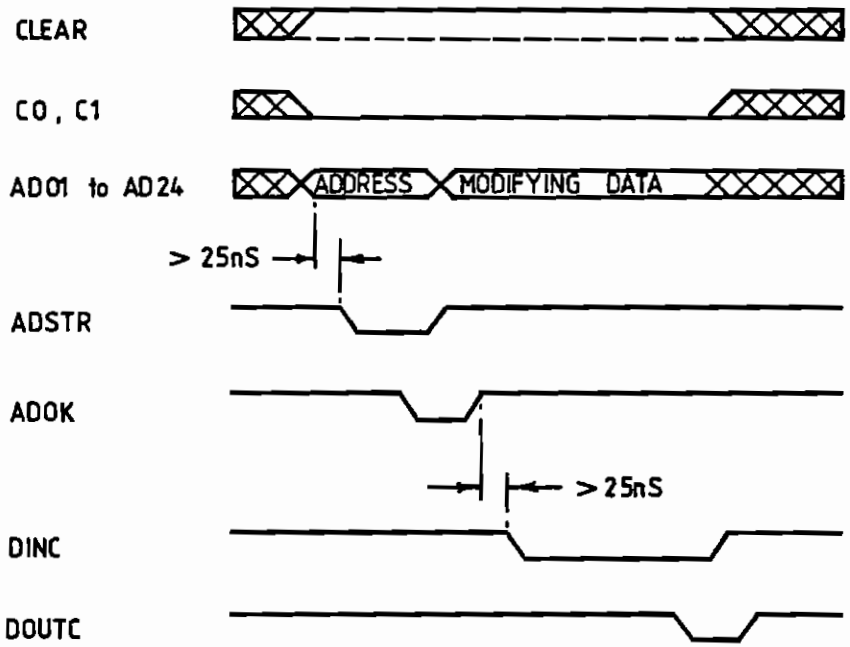
CLEAR
CO , C1
AD01 to AD24
ADDRESS
MODIFYING DATA
> 25nS
ADSTR
ADOK
> 25nS
DINC
DOUTC

FIG 4

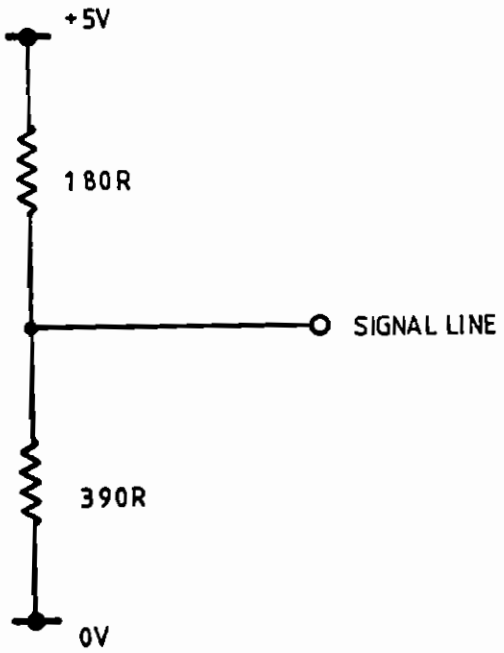
+5V
180R
SIGNAL LINE
390R
0V

FIG 5