technical memorandum Daresbury Laboratory

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A PROGRAMMABLE WAVEFORM GENERATOR

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1. INTRODUCTION

In an electronics laboratory a need exists for a voltage waveform generator, capable of producing a range of repetitive waveforms.

Commercially available generators divide broadly into sinusoidal and trapesoidal generators, the former generating modulated or unmodulated sine waves or bursts of sinewaves, and the latter is usually capable of generating waveforms with variable linear rise and fall times. To use a combination of the two linear circuits described would present problems. A much simpler solution is achieved by using digital techniques, in which a Random Access Memory (RAM) containing the digital format of the waveform is incremented, the output of which drives a Digital to Analogue Converter (DAC) which reconstructs the waveform.

This note describes a CAMAC based programmable waveform generator capable of producing a wide variety of waveforms, limited only by the size of the internal memory and resolution of the DAC used in the instrument.

2. PRINCIPLES OF OPERATION

The unit is based on a fast, 75 ns, cycle time RAM and a fast, 80 ns, settling time DAC.

Figure 1 shows the block diagram of the unit. The data describing the required waveform is entered through the CAMAC DATAWAY and stored in consecutive addresses of the RAM.

The data describing the waveform can be generated either from an appropriate algorithm using a short CATEX[1] program or by entering the data via a keyboard and the CAMAC DATAWAY from a predetermined list.

The memory is then sequentially scanned and the data output via the DAC and a filter amplifier. The RAM has a capacity of 128, 8 bit words from which the waveform can be reconstructed by the DAC allowing each specified point of the waveform to have a resolution of 4×10^{-3}.

Figures 2-7 show a selection of waveforms obtained from the module, fig.8 is a listing of a CATEX program used to generate the gaussian pulse shape in fig.7.

3. CIRCUIT DESCRIPTION

A typical waveform would be generated as follows; data describing the waveform, up to 128 bytes is entered into the units RAM via the CAMAC DATAWAY by a F16 A0 command where, bits 1 to 8 is the data describing the height of the waveform at a given point and bits 9-15 is the position of the data in the waveform. The advantage of this is to enable quick modification of any part of the waveform.

On the output command F17 A0 bit 2 the on board clock is enabled. The rate of conversion for each of the 128 samples is set by a front panel switch, this can be either 10 MHz or 1 MHz.

The mark to space ratio is selectable from the front panel, a range of 1:1, 1:10, 1:100 and continuous are possible. This is accomplished by disabling the clock gate for a set period this leaves the address counter pointing to the last location in the cycle, therefore the level of output during the space is determined by the value stored in the last location.

The RAM comprises of 16 integrated circuits, each with sixteen addresses four bits wide. The address counter points to sequential addresses in the RAM, when addressed the data is read out into a latch. The latch is incorporated as the data takes time to settle and so would give false codes to the DAC. Data is not clocked into the latch until all bits have settled, it is then passed to the DAC. The DAC gives a step representation of the data in analogue form. A low pass filter amplifier follows the DAC to give a 0 to 1 V output waveform.

4. LINEARITY

The system shown in fig.9 was used to measure the linearity of the unit. Under computer control the unit was programmed to generate voltage

levels which were measured by a programmable digital voltmeter. The measured results were compared with the programmed values to give the difference error.

Figure 10 shows the difference error of each bit where bit 0 represents all bits off (offset error) and bit X represents all bits on (full-scale error).

Figure 11 shows the errors of all 256 voltage levels. The linearity errors are given by

$$Er = \frac{Vm - Vp}{Vfs} \times 100\%$$

where Vm = measured voltage
Vp = programmed voltage
Vfs = fullscale voltage

The maximum linearity error was 0.2%, this is 1/2 the least significant bit.

5. CONCLUSIONS

Analogue signals with a 1 V peak amplitude and 4 mV resolution can be generated, each signal can be defined by up to 128 points.

Varying the clock frequency and controlling the mark to space ratio enables pulse periods from 12.8 µs to 12.8 mS to be obtained.

Better amplitude resolution could be achieved by using a higher resolution DAC and longer word length memory. Better timing resolution could be obtained by adding more memory.

6. ACKNOWLEDGEMENTS

I wish to thank Dr. M.M. Przybylski for help during the project and Mr. G. Hughes for correcting the manuscript.

7. REFERENCES

1. CATEX version 1 15th September 1980, Daresbury Laboratory

APPENDIX A

Specification

Outputs:

Front panel Bnc	-	0 to 1 V
Impedance	-	50 Ω
Linearity	-	± 2 mV
Resolution	-	4 mV
Min. Risetime	-	250 ns
Pulse width	-	0.6 µs to 128 µs
Repetition period	-	12.8 µs and 128 µs Continuous mode
	-	25.6 µs to 12.8 ms mark to space mode

Inputs:

Data	-	8 bits - from CAMAC dataway
Address	-	7 bits - from CAMAC dataway
Rate	-	1 MHz, 10 MHz - front panel selectable
Mode	-	mark to space, continuous - front panel selectable
Mark to space settings	-	1:1, 1:10, 1:100

CAMAC Commands

F16 A0 - Bits 1-15	-	write to RAM
F17 A0 - Bit 1	-	disable clock
Bit 2	-	enable clock
Bit 3	-	reset module

FIGURE CAPTIONS

Fig.1 Block diagram of unit.

Fig.2 Sinewave output waveform 12.8 µs period.

Fig.3 Step function output waveform.

Fig.4 Ramp function output waveform.

Fig.5 Triangular function with mark to space 1:1 output waveform.

Fig.6 Exponential decay output waveform.

Fig.7 Gaussian pulse shape output waveform.

Fig.8 CATEX program to produce data for Gaussian pulse.

Fig.9 Block diagram of linearity test equipment.

Fig.10 Linearity error of significant bits.

Fig.11 Linearity error of all 256 data levels.

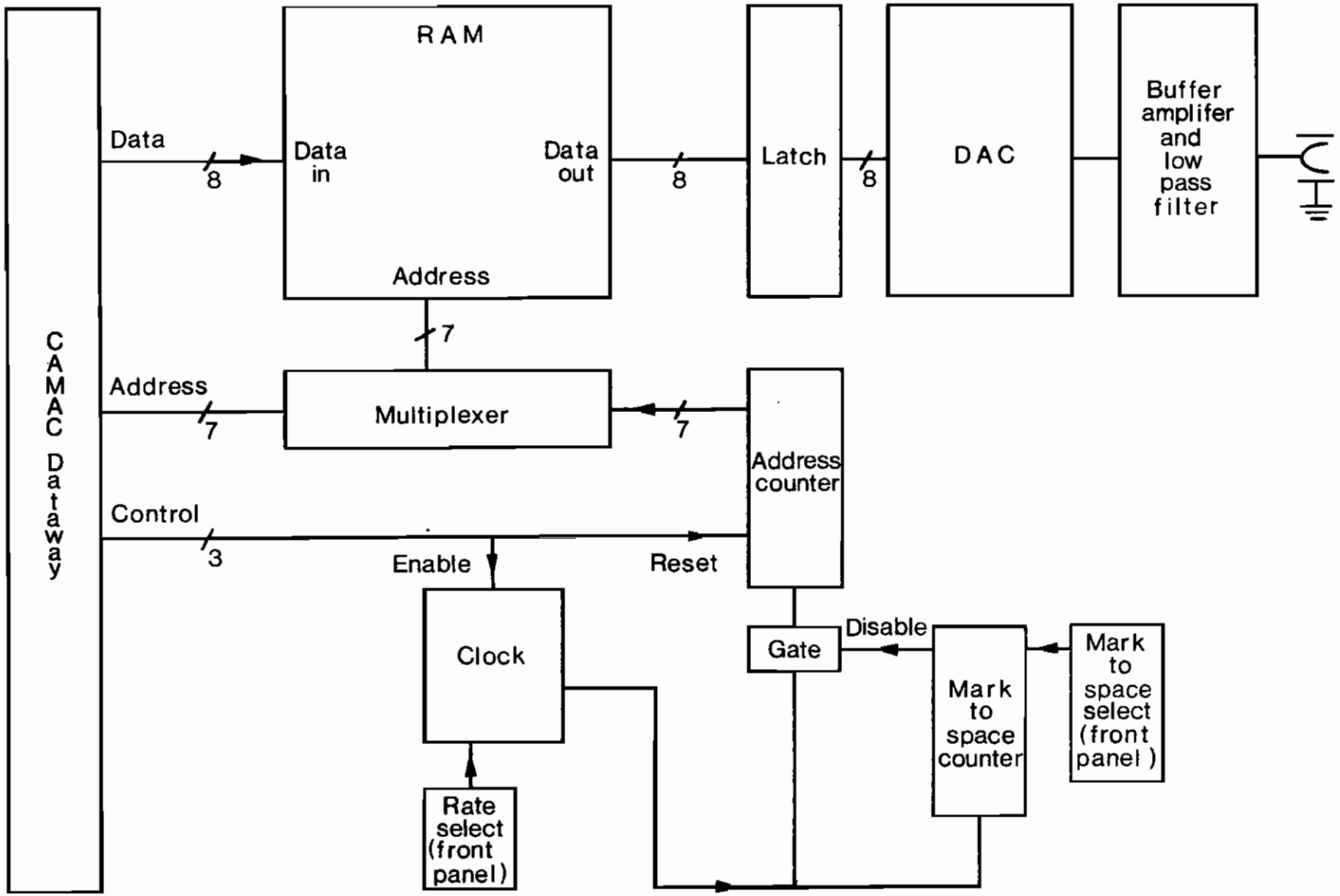

CAMAC Dataway
Data
8
RAM
Data in
Data out
Address
7
8
Latch
8
DAC
Buffer amplifer and low pass filter
Address
7
Multiplexer
7
Address counter
Control
3
Enable
Reset
Clock
Rate select (front panel)
Gate
Disable
Mark to space counter
Mark to space select (front panel)

Fig. 1

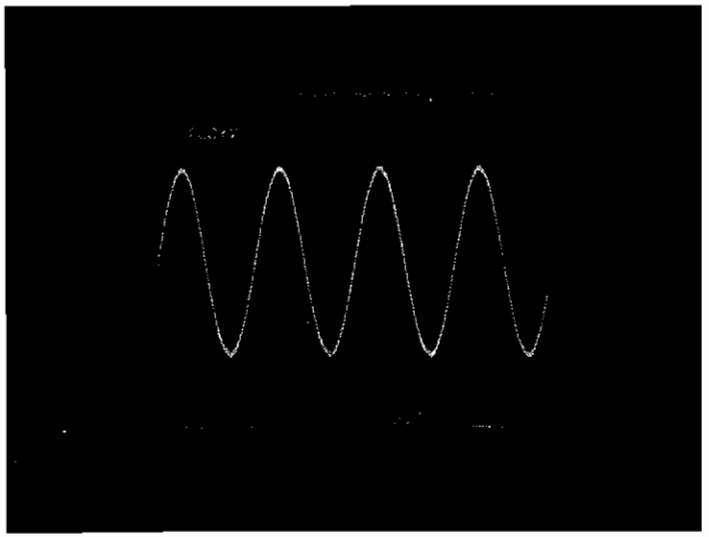


Fig.2

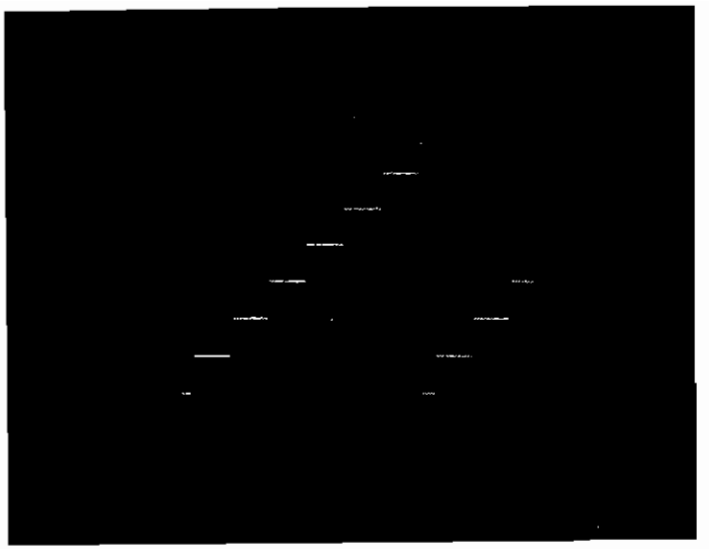


Fig.3

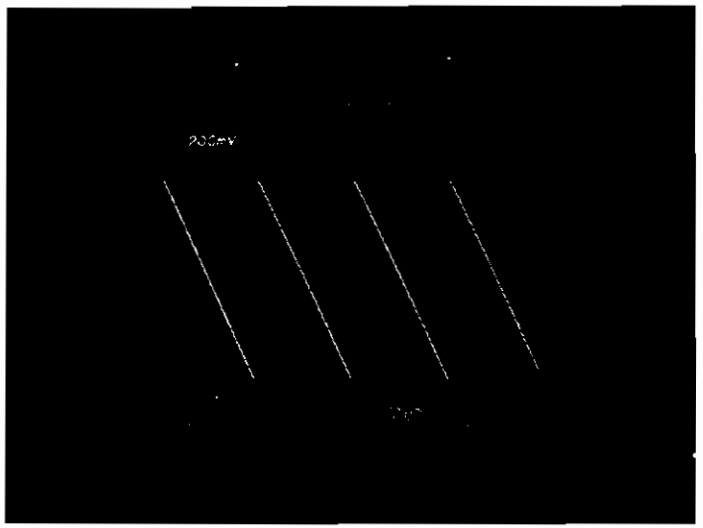


Fig.4

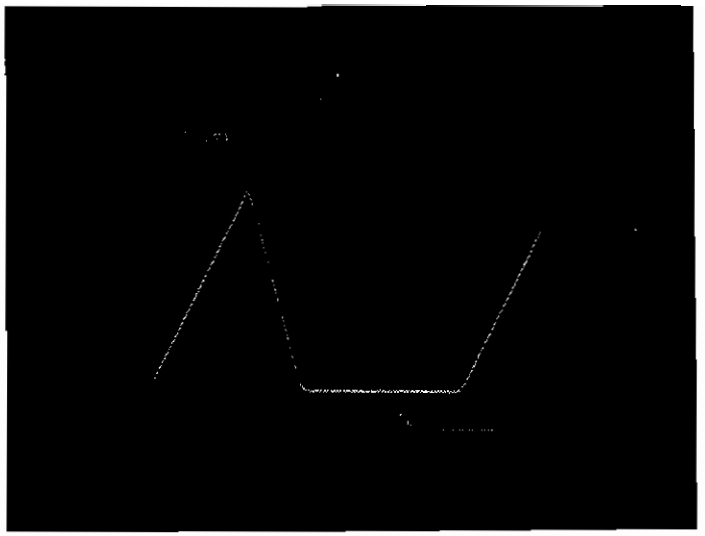


Fig.5

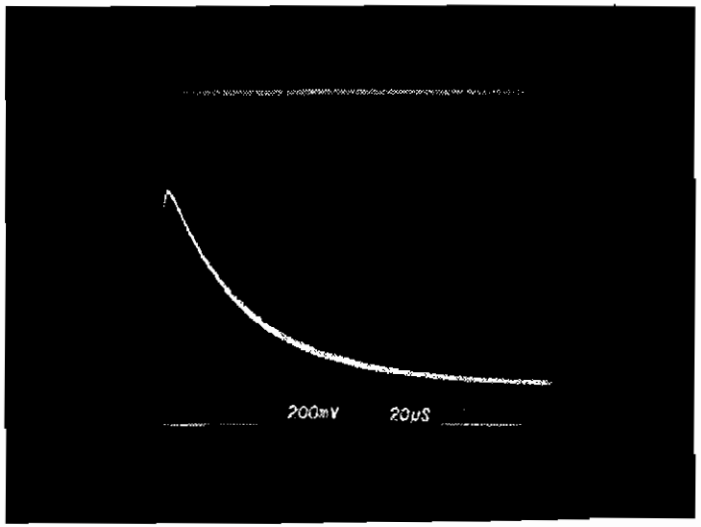


Fig.6

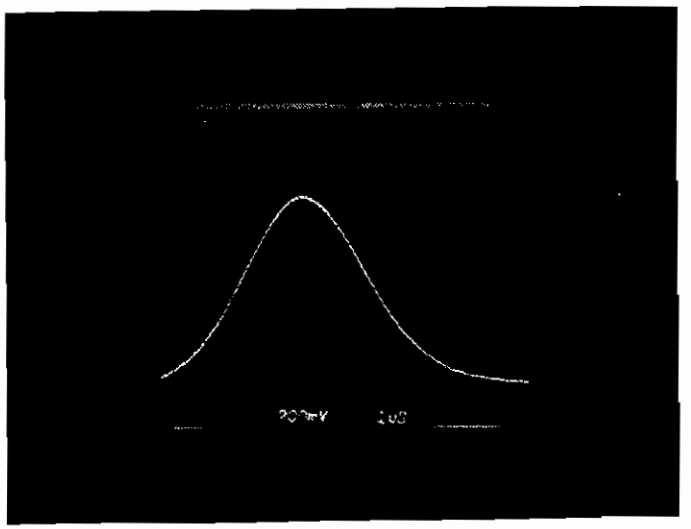
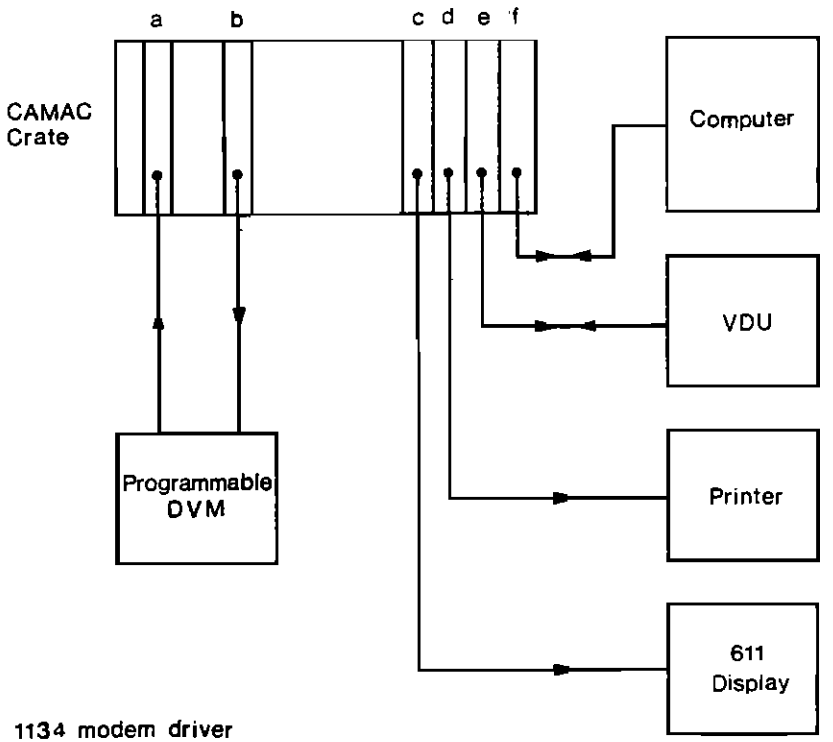


Fig.7

```
+IPA

    5
   10 DIM A(128)
   20 REAL4 B,C,D
   30 PWG=1,1,15
   40 FOR I=-63 TO 64
   50 LET B=I2TOR4(I)
   60 LET B=B/20
   70 LET B=EXP(-B*B)
   80 LET B=B*255
   90 LET J=I+64
  100 LET A(J)=R4TOI2(B)
  105
  110 LET A(J)=A(J)+(J*256)
  120 WT1 PWG,1,A(J)
  130 NEXT I
+
```

Fig.8



a. 1134 modem driver
b. Programmable waveform generator
c. 7011 611 display driver
d. 7061 teletype interface
e. 7061 teletype interface
f. EC372A crate controller

Fig. 9

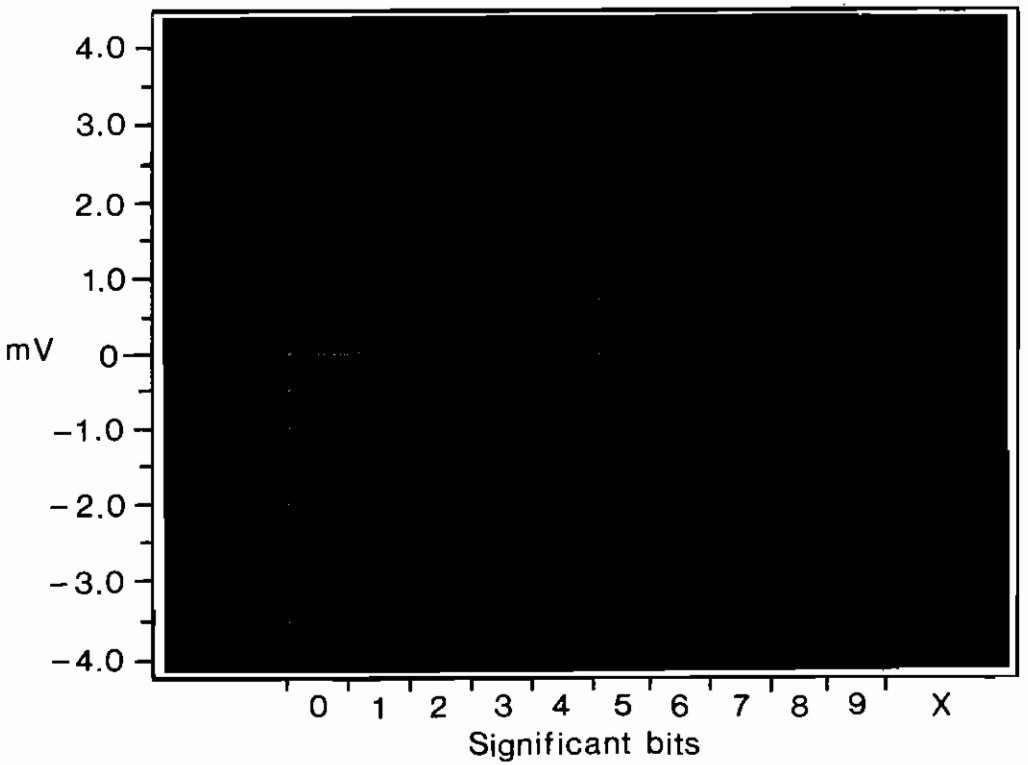


Fig. 10

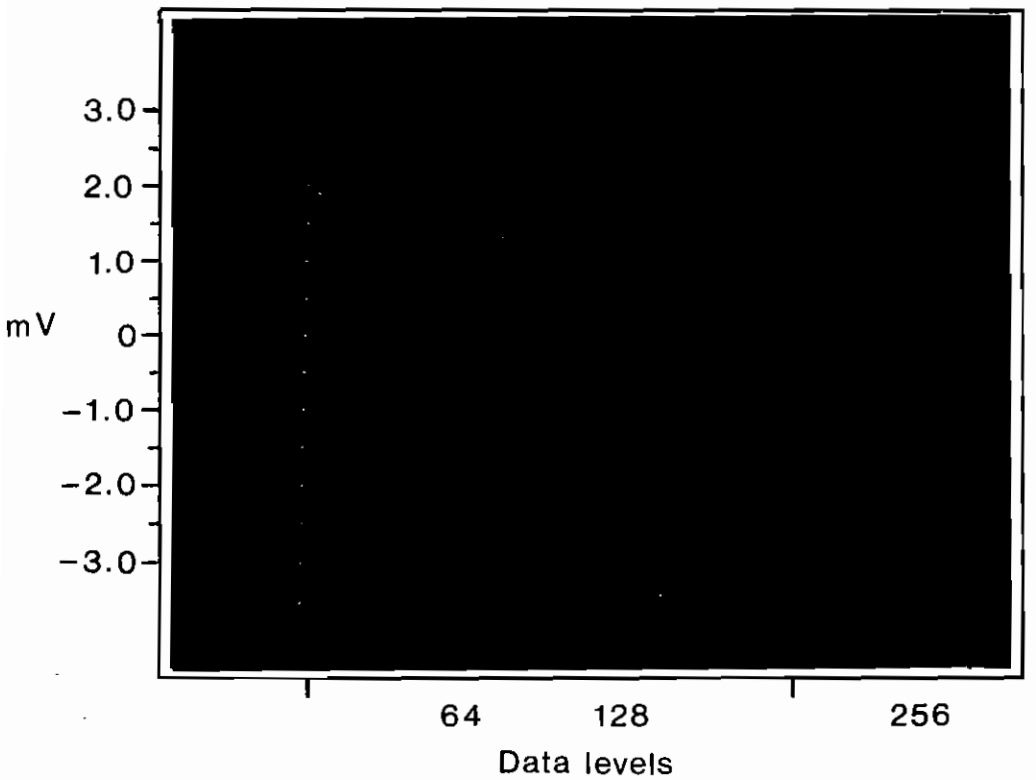


Fig. 11