technical memorandum Daresbury Laboratory

DL/CSE/TM22

DATA RATE MEASUREMENTS ON THE NSF DATA ACQUISITION STATIONS

by

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NOVEMBER, 1982

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1. INTRODUCTION

This memorandum presents the results of measurements taken on the NSF data acquisition stations to determine the maximum rates at which multi-parameter event data can be collected. It is already known that the Event Manager and CAMAC readout processor (Read and Store Controller) can acquire data at a peak rate far in excess of that at which the data can currently be transferred into the data handling processors (approximately 500,000 and 100,000 ADC values per second, respectively). This allows the Read and Store Controller to act as a de-randomising buffer between the experiment and the processors. However, the measurements presented here indicate the maximum rates that can be achieved using the present design philosophy of an Event Manager driving a CAMAC readout system. To this end the following are assumed:

1) Data is only read into the Read and Store Controller. (A modified unit could then pass this directly to the processors - obviating the need for it to pass over the CAMAC dataway a second time as in the present system.)
2) The Read and Store Controller has unobstructed use of the CAMAC dataway, i.e. the present 'Singles' histogramming is not taking place.
3) All ADCs involved in verified events proceed to convert normally, i.e. no events fail (as these would contribute to event processing time without contributing to collected data).

2. EVENT MANAGER OPERATION

This section reviews the operation of the Event Manager to explain the delays involved in processing an event. A block diagram of the Event Manager and its connections to the CAMAC readout system and to the ADCs is shown in fig.1. Figure 2 is a flow diagram of the operations involved in processing an event, which are also described below.

The 18 event triggers are accepted and verified in parallel and in real time, but the subsequent ADC conversion monitoring and readout processes are done in series (with a certain degree of parallelism, as mentioned later). Once an event has been verified it is put in a queue with other verified events until the rest of the Event Manager is free to process it. This processing involves four routines in the EMP (Event Manager Processor) board:

2.1 TW routine

(The TW signal indicates that a trigger is waiting for processing.) This transfers the ADC pattern for the event from the appropriate trigger register to the ADC-conversion monitoring register.

2.2 CCC routine

(Conversion Cycle Complete.) This transfers the ADC pattern to a holding buffer, thus freeing the conversion monitoring register for other events.

2.3 RCI routine

(Readout Cycle Initiate.) This transfers the ADC pattern to the Read and Store Controller to initiate event readout, and also to the readout monitoring register.

2.4 RCC routine

(Readout Cycle Complete.) This routine simultaneously clears all ADCs involved in the event.

Each routine is initiated by status signals indicating 'Conversion Cycle Complete', etc. - if the appropriate destination for the ADC pattrn is free. Event processing is done in parallel in that one event can be in

the readout phase, while another is held in the buffer (waiting for the Read and Store Controller to become available) and a third is in the conversion monitoring phase.

3. MEASURED TIMINGS

The measured timings for a single event passing through the system are shown in the timing diagram, fig.3. These include the times for the EMP routines and various other system delays. Together these determine the total processing time for a single event: (14.6 + 1.9 n) microseconds, where n is the number of ADCs in the event. Note that if an ADC takes longer than 4.5 microseconds to convert the extra time will add directly to the event total.

4. TIMINGS FOR MULTIPLE EVENTS

From the timings for a single event the timings for multiple events can be worked out as illustrated in fig.4, which is for 2 events of 3 ADCs each. It is assumed that a trigger input is verified sufficiently soon after the associated ADCs have been cleared (following the previous event) for processing to be continuous. The time in which a trigger must be generated to achieve this is shown in fig.4; it will increase with increasing numbers of events and ADCs.

Note that some of the synchronisation delays shown in fig.3 do not contribute to the timings calculated in fig.4 as they overlap with the execution of routines. In addition the TW and CCC routines can run in parallel with the readout of ADCs by the Read and Store Controller. Thus the time between completing the readout of successive events, plotted in fig.5, reduces to (5.5 + 1.9 n) microseconds for n = 3 or more ADCs per event. 5.5 microseconds is essentially the time for the RCC and RCI routines, which cannot be done in parallel with ADC readout.

The data of fig.5 is re-plotted in fig.6 to show the period of each event-type individually (i.e. the time between acceptance of successive triggers at a particular trigger input). This nicely illustrates the effect of overlapping conversion and readout in that the periods for 1 and 2 event-types is not greatly different when using a small number of ADCs. As the number of ADCs increases the readout time starts to dominate so that the ratio of periods tends to 2:1, as expected.

The same data is plotted again in fig.7 as the rate of data collection in (16-bit) words per second. The event header word is included, thus the data rate is $\left\{\frac{n + 1}{14.6 + 1.9\ n}\right\}$ for one event type, and $\left\{\frac{n + 1}{5.5 + 1.9\ n}\right\}$ for two or more event types of 3 or more ADCs each.

5. READ AND STORE CONTROLLER TIMINGS

Finally it is interesting to note how the Read and Store Controller's readout period of 1.9 microseconds is constituted. As mentioned earlier no other controller was attempting to use the dataway, and the Read and Store Controller had 'Request' directly connected to 'Grant In'. The ADC interfaces were situated in a remote crate so that the Controller had to access these via the Daresbury Link System.

Arbitration period	170 ns
Link arbitration and delays	410 ns
Minimum auxiliary controller CAMAC cycle	1100 ns
Read and Store overheads	220 ns
	1900 ns

FIGURE CAPTIONS

Fig.1 Event Manager and CAMAC Block Diagram

Fig.2 Steps involved in processing an event.

Fig.3 Single ADC, Single Event Timing

Fig.4 Processing 2 Event-Types (3 ADCs per event).

Fig.5 Event processing times

Fig.6 Event repetition times (for each event-type individually).

Fig.7 Data collection rates.

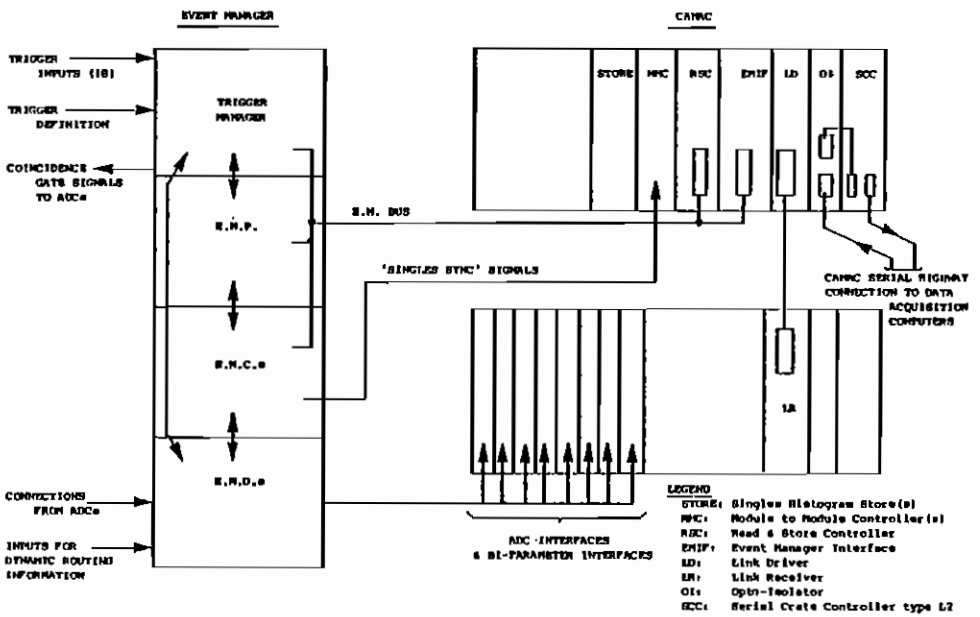
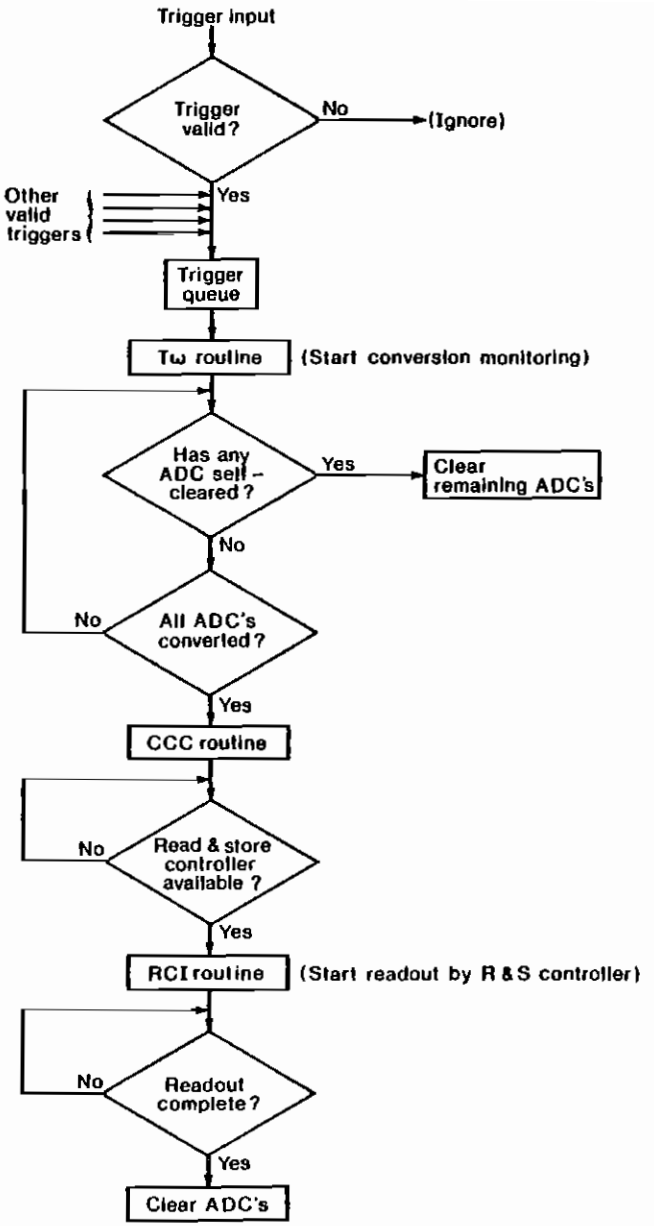
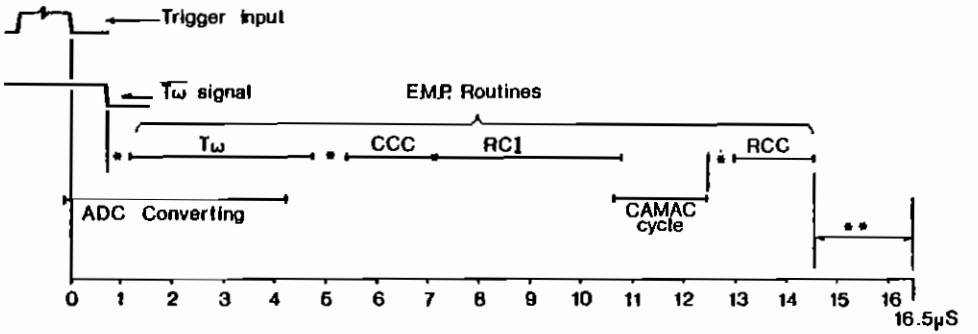


Fig.1



Steps involved in processing an event

Fig. 2

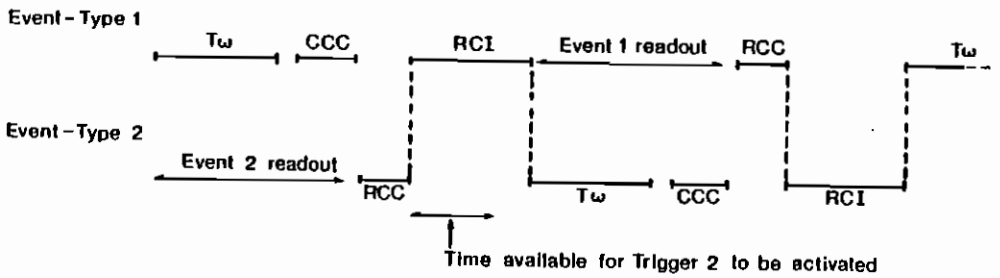


* Signal synchronisation times on EMP board

** ADC recovery and Trigger set-up times

Single - ADC, Single - Event timing

Fig. 3



Processing 2 Event-Types (3 ADC's per event)

Fig. 4

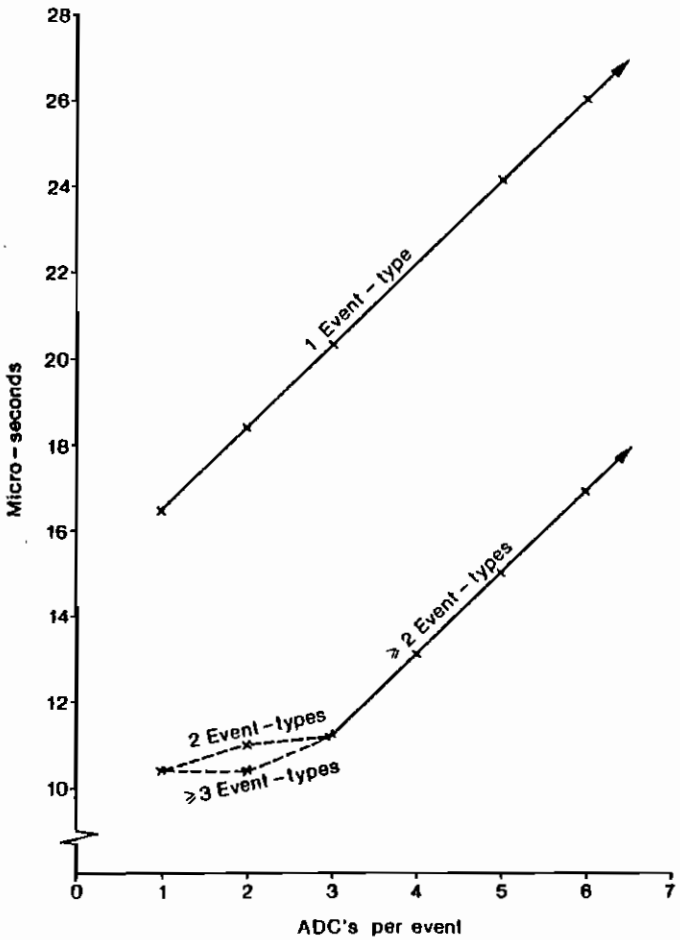


Fig. 5

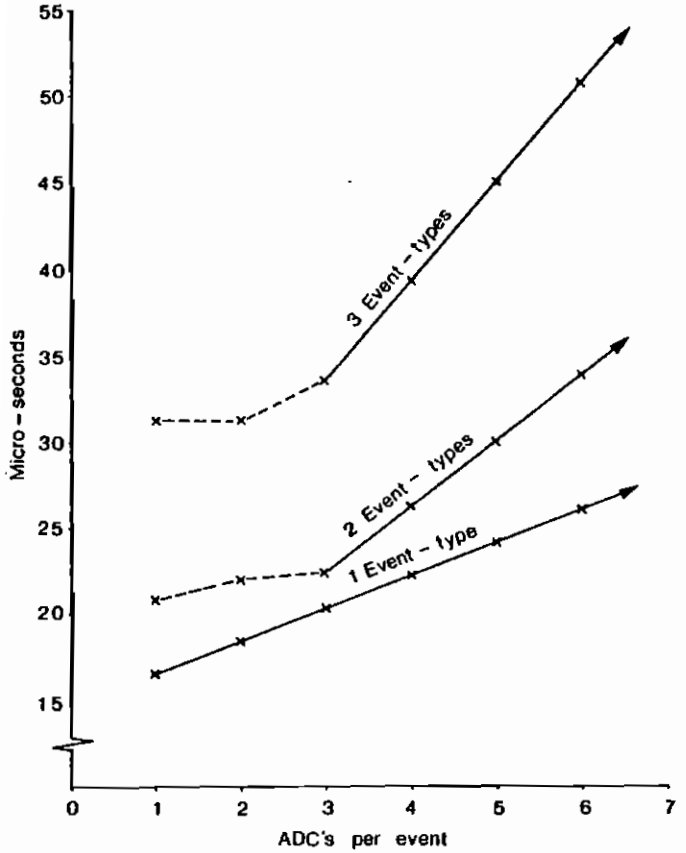

Micro - seconds
55
50
45
40
35
30
25
20
15
0
1
2
3
4
5
6
7
ADC's per event
3 Event - types
2 Event - types
1 Event - type

Fig. 6

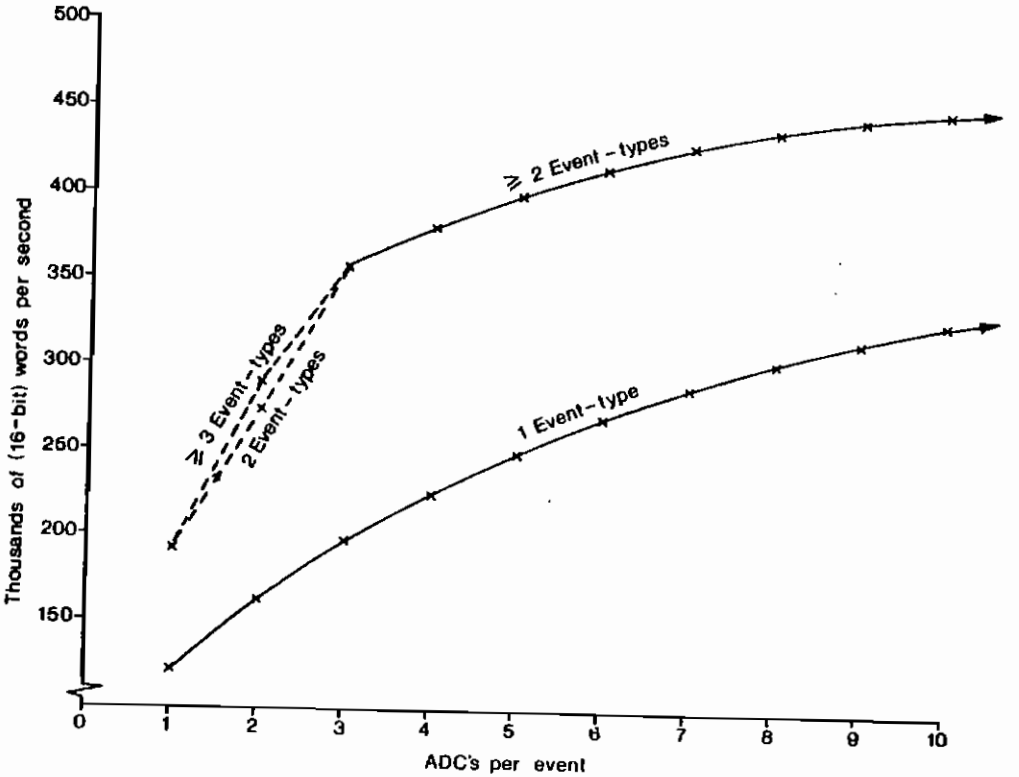

Thousands of (16-bit) words per second
500
450
400
350
300
250
200
150
0
1
2
3
4
5
6
7
8
9
10
ADC's per event
≥ 3 Event - types
2 Event - types
≥ 2 Event - types
1 Event - type

Fig. 7