Technical Report
RAL-TR-1998-053

CLRC

A Guide to Time Resolved Neutron Diffraction

S J Payne and M Hagen

5th August 1998

COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS

Enquiries about copyright, reproduction and requests for additional copies of this report should be addressed to:

The Central Laboratory of the Research Councils
Library and Information Services
Rutherford Appleton Laboratory
Chilton
Didcot
Oxfordshire
OX11 0QX
Tel: 01235 445384 Fax: 01235 446403
E-mail library@rl.ac.uk

ISSN 1358-6254

A GUIDE TO TIME RESOLVED NEUTRON DIFFRACTION MEASUREMENTS USING THE TRS SYSTEM AND SOFTWARE

S. J. Payne and M. Hagen

Department of Physics, Keele University, Staffordshire, ST5 5BG, UK

Abstract

This guide contains a description of the hardware and software constructed for the Time ReSolved (TRS) system on the PRISMA beamline. Specifically the guide contains the following. (i) An overview of stroboscopic time resolved measuring techniques using the superframe and superperiod methods. (ii) A functional description of the hardware in the TRS system. (iii) A functional description of the hardware used in a high voltage system (HVS) which can be driven by the TRS. (iv) A description of the operating system and data analysis software for the TRS. (v) An appendix which contains a detailed technical description of the TRS. (vi) An appendix which contains listings of the software programmes and macros.

Contents

1 Introduction **4**

2 The Time Resolved Technique **7**
2.1 The ISIS Data Acquisition Electronics System (DAE) 7
2.2 The Superframe Approach 9
2.3 The Superperiod Approach 11
2.4 The Software Approach 13

3 The Time Resolved System **14**
3.1 The Field Programmable Gate Array, FPGA, system 14
3.2 The Basic Functions of the TRS system 15
3.3 Functional Description of TRS System - Superframes 18
3.3.1 Possible Failures during Superframe Production 22
3.4 Functional Description of TRS System - Superperiods 25

4 The High Voltage Switch System **27**
4.1 The GHTS-100 High Voltage Switch 30
4.2 High Power Resistance Box 30
4.3 The EFA Signal Box 32
4.4 High Voltage Probe Assembly 32

5 Software for using the TRS **33**
5.1 The TRS Parameters in the PRISMA Program 33
5.2 The EON Parameter 34
5.3 The DELAY Parameter 34
5.4 The DURAT Parameter 35
5.5 The SFRAM Parameter 35
5.6 LWIN and UWIN - The Window Limit Parameters 36
5.7 The HARDPERIODS.DAT file 36
5.8 The ToF parameters in the PRISMA program 38
5.9 Data Analysis GENIE Macros 39
5.9.1 TDD4:==@PRISMA_KNH_COM:TSPACE4.COM 39
5.9.2 ASF4:==@PRISMA_KNH_COM:ANATIM.COM 40
5.9.3 ASP4:==@PRISMA_KNH_COM:ANAPER.COM 42
5.10 The Diagnostic Programmes REGRED and REGSET 43

A Circuit Diagrams **44**
A.1 The Xilinx Schematics 44
A.2 Register Control and Clock Distribution 46
A.2.1 Clock Distribution 46
A.2.2 Data Load/Read 46
A.2.3 Data Register '2164' 48
A.3 System Control 50
A.3.1 Operation 50
A.3.2 The IOFF signal 52
A.4 Limit Generator System 53

A.4.1 The Lower Limit Circuit . . . 55
A.4.2 The Upper Limit Circuit . . . 56
A.4.3 Frequency of the Limit Pulses . . . 56
A.5 The Comparator System . . . 56
A.5.1 Operation - Superframe Pass . . . 58
A.5.2 Operation - Superframe Fail . . . 59
A.5.3 Synchrotron Failure . . . 59
A.6 The Superframe Register . . . 60
A.6.1 Operation - Superframe Mode . . . 60
A.6.2 Reset Procedure - Superframes . . . 62
A.6.3 Operation - Superperiod Mode . . . 63
A.6.4 Special Functions . . . 63
A.7 External Field Control System . . . 64
A.7.1 External Field Delay Circuit . . . 64
A.7.2 The EFA Length Control Circuit . . . 67
A.7.3 Control Options . . . 67
A.7.4 EFA Delay and Length Step Size . . . 67
A.8 Watchdog System . . . 68
A.8.1 The WDOG_A Circuit . . . 68
A.8.2 The WDOG_B Circuit . . . 70

B Programmes and Macros **71**
B.1 The RUNTRS and OFFTRS Subroutines . . . 71
B.2 The HWRIT Program . . . 76
B.3 The TDD4 Macro . . . 77
B.4 The ASF4 Macro . . . 80
B.5 The ASP4 Macro . . . 82
B.6 The STOFIL Program . . . 83
B.7 The TRSORT Program . . . 84
B.8 The TRAVER Program . . . 85
B.9 The Diagnostic Programmes . . . 86
B.9.1 The REGRED Program . . . 86
B.9.2 The REGSET Program . . . 87
B.9.3 The REGLINK Link Command . . . 89

1 Introduction

The pulse structure of a synchrotron based neutron source such as ISIS can be used to carry out stroboscopic real time (time resolved) neutron diffraction studies of a sample. An example of such a study would be a phase transition which is not driven by changes in temperature but instead by the controlled application of some external field which is synchronised to the production of the neutron pulses. At ISIS this synchronisation is achieved by making use of an electronic signal, a 400ns "master" pulse (see next section), which indicates the time when a neutron pulse leaves the target and moderator station. Using this pulse and a knowledge of the neutrons time of flight it is possible to calculate the time at which the neutrons will arrive at the sample and therefore a time at which to apply the external field. By using this technique with a range of (delay) times for the application of the external field, it is possible to map out the real time behaviour of the scattering cross section and hence also the sample.

The procedure described above is shown schematically in figure 1 for the situation of Bragg peak scattering from the (h, k, l) planes of a single crystal. The neutrons are produced at the moderator at time T=0 indicated by the origin of the axis in the figure. The geometry of the spectrometer is such that the sample is a distance L_i from the moderator and L_f from the detector which itself is at a scattering angle ϕ with respect to the incident neutrons. If the Bragg peak wavevector is Q_{hkl} then using Braggs law,

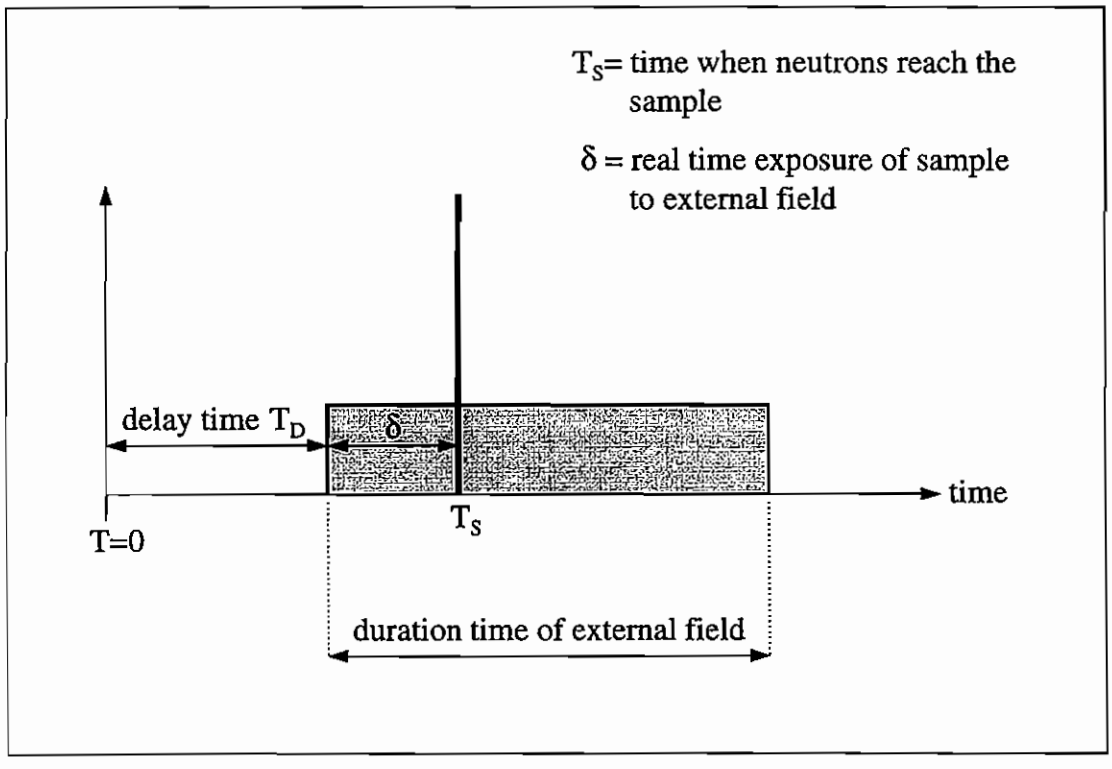

Figure 1: A schematic representation of the stroboscopic time resolved technique. An external field is applied to the sample at a time δ before the neutron pulse reaches the sample at time T_S.

$Q = 2k \sin \frac{|\phi|}{2}$, de Broglies law $p = \hbar k$ and the equation $k = m_N L/\hbar T$, the time T_B at

which the neutrons scattered from the *hkl* planes arrive at the detector is

$$\mathrm{T_B} = \frac{2m_N(L_i + L_f)}{\hbar}\left(\frac{\sin\frac{|\phi|}{2}}{Q_{hkl}}\right) \tag{1}$$

Now the time $\mathrm{T_S}$ at which the neutrons are at the sample is

$$\mathrm{T_S} = \left(\frac{L_i}{L_i + L_f}\right)\mathrm{T_B} = \frac{2m_N L_i}{\hbar}\left(\frac{\sin\frac{|\phi|}{2}}{Q_{hkl}}\right) \tag{2}$$

Hence if the external field is applied at a delay time $\mathrm{T_D}$ after the ISIS neutron pulse was produced the measured Bragg peak will correspond to the behaviour of the sample at a real time δ after the field was applied which is given by

$$\delta = \mathrm{T_S} - \mathrm{T_D} = \frac{2m_N L_i}{\hbar}\left(\frac{\sin\frac{|\phi|}{2}}{Q_{hkl}}\right) - \mathrm{T_D} \tag{3}$$

which can be very simply re-arranged to give the delay time through the formula

$$\mathrm{T_D} = \frac{2m_N L_i}{\hbar}\left(\frac{\sin\frac{|\phi|}{2}}{Q_{hkl}}\right) - \delta \tag{4}$$

The process described above is a stroboscopic process during which the sample will both respond to the application of an external field and then relax back again once the field is removed with certain intrinsic response and relaxation times. During such a stroboscopic process the external field would normally be applied for a duration time that is long enough to allow the sample to fully respond to the applied field. Similarly it is desirable that the sample should fully relax after the field has been removed before the sample is then strobed again. Normally at ISIS neutron data is collected and stored during the 20ms period between neutron pulses, which is known as one ISIS frame. However a facility has to be available in real time stroboscopic experiments to measure those samples whose response to, or relaxation from the application of the external field in real time is longer than the time offered by a single ISIS frame. One approach to measurements on samples that fall into this category is to "daisy chain" ISIS frames together to form a single *superframe* whose length will allow the particular transition under study to be fully cycled ensuring that the sample is in an identical state at the start of each superframe. To accomplish the above, additional electronics had to be added to the instruments (i.e. PRISMA's) data acquisition electronics (DAE) which is normally responsible for storing the neutron data only in the form of single 20ms ISIS frames, as detailed in the next section. The additional electronics was designed to instruct the DAE to store in a single block of memory whole superframes of up to 440ms duration and to sum together these superframes in the same way that ordinary 20ms ISIS frames are summed. Also, this extra electronics uses the ISIS master pulse as a reference signal to correctly time the application of the external field to the sample.

The first real time experiment using this technique at ISIS involved a high voltage electric field synchronised to the neutron pulse production. This experiment [1] investigated the transient properties of the incommensurate to commensurate ferroelectric phase

transition in Rb_2ZnCl_4 using a 8kV/cm switched d.c electric field and demonstrated the feasibility of time resolved experiments at ISIS. However the electronics that was constructed to daisy chain the ISIS frames together and to control the electric field was very limited in its capabilities and needed to be completely redesigned in order to turn it into a working system. The set of criteria that was laid out for the new system is listed below.

- All functions offered by the new system (e.g superframe length and external field control) should be software controlled by the instrument computer; the original system was manually controlled by sets of d.i.p switches.

- The programmable superframe length should be any value in the range from 2 to n ISIS frames long where n is the maximum length allowed by the DAE (n=22 (440ms)), see section 2.1); the original system would only allow superframes containing an even number of ISIS frames.

- The duration of the applied external field should be variable in small time steps (i.e. 10μs) up to the size of the superframe; in the original system the length was always half the superframe length.

- The delay time between the appearance of the master (ISIS) pulse and the application of the external field to the sample should be selectable in small time units (i.e. 10μs) allowing good resolution of the real time behaviour of the sample; in the original system the steps were quite coarse at 1ms steps. Though finer steps could be achieved this could only be done by altering the scattering angle of the incident neutrons and hence the scattering conditions.

- The system must test that the 20ms ISIS pulses which form the superframe maintain their 20ms periodic time (within a tolerance set by the instrument control computer). If they do not the new system must reject the superframe and cause the DAE to reject any data collected during that superframe; the original system was unable to do this.

- The new system must be able to detect a synchrotron failure and (a) halt the production of the superframes (b) reject data collected during the current (incomplete) superframe and (c) switch off the external field to the sample. The system must be able to restart automatically once the synchrotron is functioning normally again; this was outside the scope of the original system.

The next section in this chapter describes the time resolved technique itself. Initially it describes how the DAE stores neutron data and highlights limitations within the DAE which had to be taken into account. The section also covers 3 different approaches that can be used when conducting time resolved experiments at ISIS using the TRS system. The choice of approach depends on the time needed to cycle the phase transition under investigation. The last section, section 3, describes the new TRS system, how it is constructed and how it is able to use the master pulses to not only control data collection within the DAE but also the application of an external field to a sample.

2 The Time Resolved Technique

There are three approaches to performing time resolved experiments at ISIS and the choice of which approach is used is determined by the total time taken by a sample to fully respond to the applied field and then completely relax back again. If this total time to cycle the phase change in the sample is referred to as T_{cyc} then these three approaches are as follows;

- superframe approach - when T_{cyc} is less than 440ms,
- superperiod approach - when T_{cyc} is between 440ms and 21 minutes,
- software approach - when T_{cyc} is greater than 21 minutes.

In the following subsections these approaches are described in general terms. However since both the superframe and superperiod approaches are inextricably linked with the operation of the ISIS data acquisition system, the DAE, the operation of the DAE system is described first.

2.1 The ISIS Data Acquisition Electronics System (DAE)

The data acquisition electronics system is that part of the PRISMA instrument which is responsible for collecting and storing all the time of flight data that it receives during each 20ms ISIS frame. This data is in the form of counts from the 16 ^{3}He gas detectors and two scintillator monitors used on PRISMA. The DAE can only collect time of flight data if it knows when each ISIS frame starts. The start of an ISIS frame is defined as the time when the neutrons leave the target station, i.e. the time at which the neutron pulse was produced. The way that this is achieved is shown schematically in figure 2. As the proton pulses from the synchrotron travel to the target station they pass through the proton pulse sensor. This sensor produces a single 400ns wide positive master (ISIS) electronic pulse for each proton pulse that passes through which is then sent to the DAE. The time difference between the production of this ISIS pulse and the actual production of the neutron pulse is extremely small and they can then effectively be considered as the same event. This ISIS pulse is used as a reference signal from which to measure the neutrons flight time since this pulse effectively indicates the time at which the neutrons left the target station.

Once the neutron counts from the ^{3}He detectors (and discriminator electronics) arrive in the DAE they are stored into memory. This memory can be thought of as a histogram of counts for a sequence of time bins or time channels. These time channels can be as small as 1μs in width, although they can be made larger if required, and correspond to addresses for different locations in the DAE memory. As the counts arrive at the DAE the relevant (time channel) locations in the memory, corresponding to the time the count arrived with respect to the start of the ISIS frame, are then updated. If 1μs time channels are used a 20ms ISIS frame would require a total of 20000 time channels in the DAE memory for each detector and monitor. For the normal critical scattering and inelastic spectroscopy experiments the DAE electronics and memory system is well able to cope with the demands made on it. However in a real time experiment it is necessary to go beyond 20ms and as a consequence certain limits on the performance of the DAE electronics become apparent which are not normally a problem. Firstly the

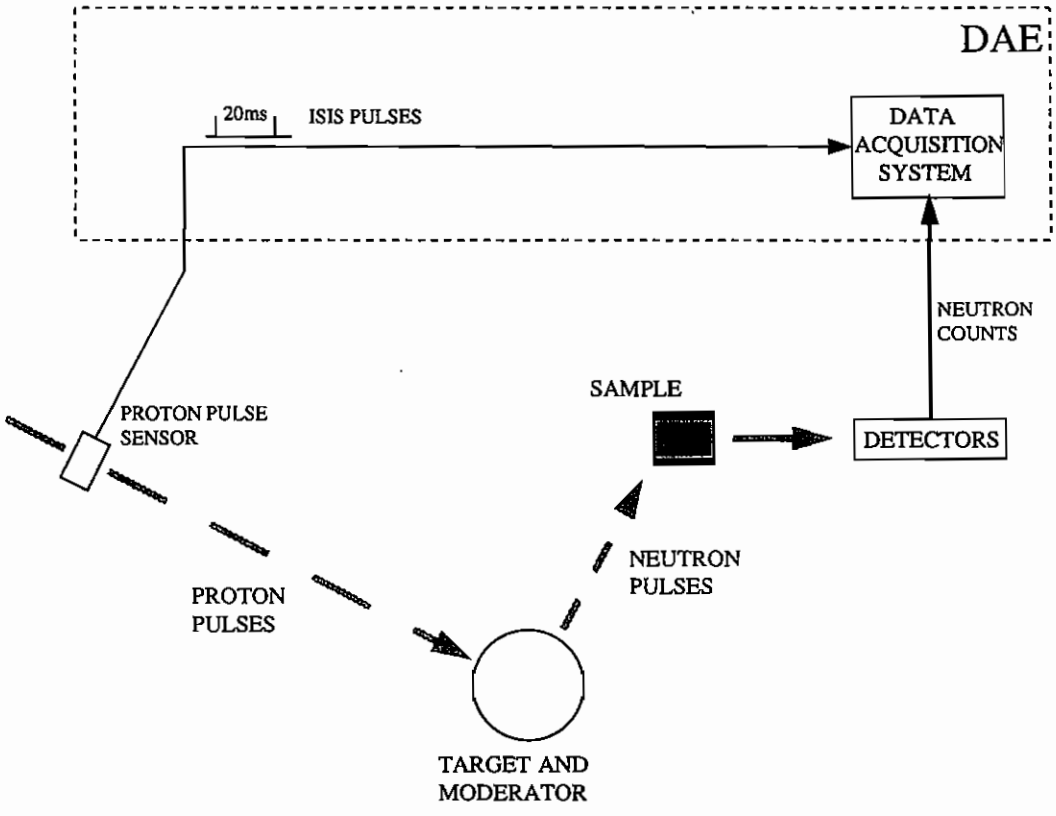

Figure 2: Figure showing the production of the proton extraction pulse, the ISIS pulse, which is sent to the DAE to control the time of flight electronics and the storage of the time of flight data received from the detectors.

time channel generator (TCG) electronics can only generate a maximum of 32000 time channels. Thus this limits the maximum framelength using $1\mu s$ times channels to 32ms. To achieve longer framelengths the size of the time channels can be increased from $1\mu s$ to $2\mu s$ for framelengths of less than 64ms duration, from $2\mu s$ to $3\mu s$ for framelengths less than 96ms and so on. Of course this process cannot continue endlessly. The timing system within the DAE (for the neutron counts and time channel boundaries) is based around a 32MHz oscillator which leads to a fundamental time unit of 31.25ns i.e. the period time of the clock pulses from the oscillator. The normal operation of the DAE involves a frame length of 20ms and a time channel width of $1\mu s$. This width of the time channel is the period over which the time channel can receive counts. This period is normally defined as a time which is equal to 32 clock cycles of the 32MHz oscillator i.e. $32\times31.25\text{ns}=1\mu s$.

This idea of using 32 clock cycles to determine the width of each time channel is still preserved for framelengths that go beyond 32ms and which involve an increase in the size of the time channels. In this case the clock pulses from the oscillator are not used directly but instead are pre-scaled by the DAE electronics to produce a modified clock pulse with longer periodic times. Thus for example for a framelength of 40ms the DAE electronics will pre-scale the 32MHz clock by 2 producing a clock signal with a periodic time of 62.5ns. This then results in time channels of $32\times62.5\text{ns}=2\mu s$ and by using 20000 such

channels a 40ms framelength can be created. Even longer framelengths can be created in this way although there is an upper limit of 14 to the value of the pre-scaler. This upper limit means it is not possible for the DAE electronics to count to a time longer than the product of $14 \times 31.25\text{ns} \times 32 \times 32000$ time channels = 448ms. In practice the maximum allowed framelength will be 440ms because the ISIS frames are in quanta of 20ms units.

In the above discussion the storage of data in the DAE memory has so far only been considered for effectively a single frame. However frames are combined together (summed) to improve the statistics of the neutron counts. This is carried out in the DAE by a two step process, firstly a single frame of data is stored in a temporary memory location and then once the frame is complete (i.e. the next frame has been started) it is transferred from the temporary memory and summed with previously collected data within a specific permanent memory location. The data in the temporary memory location is transferred to the permanent memory using a starting address which is then incremented channel by channel. In normal instrument operation this starting address is the same for every frame. However it is possible via the hardware in the DAE to have different starting addresses for different frames. This is discussed in more detail in section 2.3.

2.2 The Superframe Approach

A superframe is produced by daisy-chaining together a string of ISIS frames to form one long frame which can then be stored within the DAE memory as single block (or string) of memory locations. The situation is shown schematically in figure 3. Normally the DAE

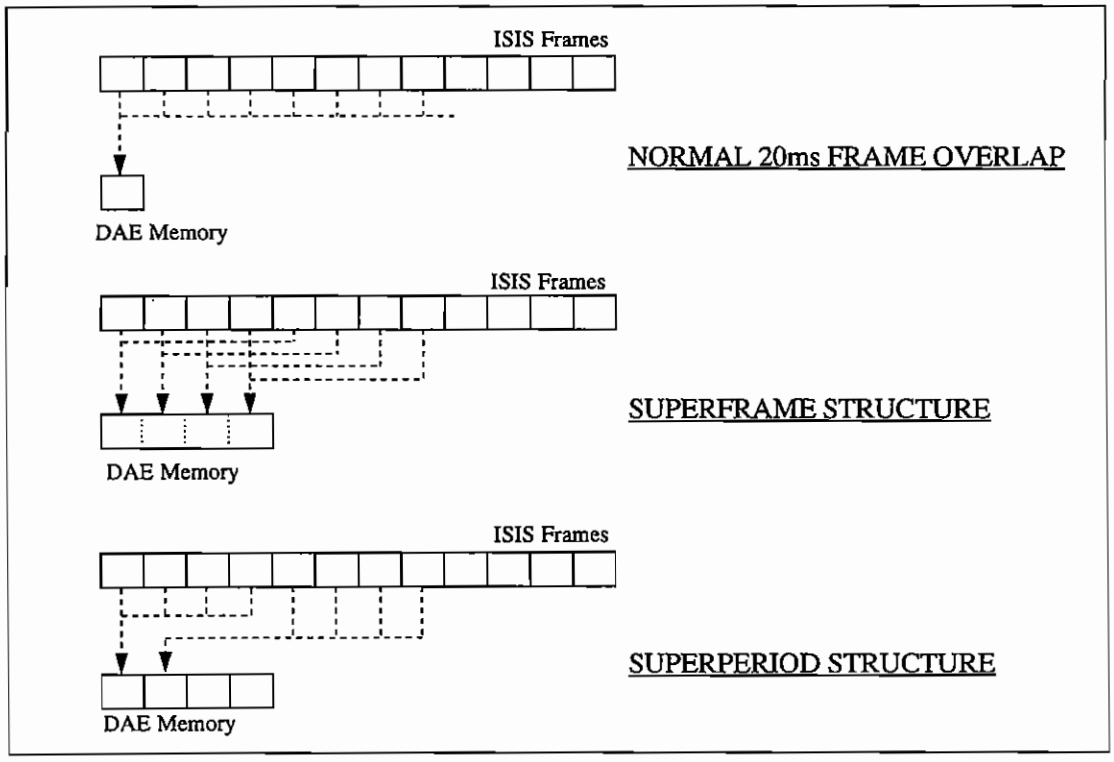

Figure 3: A schematic illustrating how the DAE stores data from single ISIS frames, superframes and superperiods into different locations within its memory as described in the text.

will ensure that the data from each 20ms ISIS frame is mapped onto the same block of

locations in its memory and it will then sum all the data together. For a superframe a daisy chain of ISIS frames (in the example of figure 3 this is 4 ISIS frames) is mapped onto a block of memory locations one after the other. At the end of the superframe the next superframe is mapped onto this same block of memory in the same way that single frames are summed together in normal operation.

During a superframe the sample is "strobed" a number of times by the pulsed neutron beam which means that the superframe contains information on the state of the sample every 20ms over the duration of the superframe. If an external field is switched on and off during the superframe then the scattering intensity, i.e. the Bragg peak intensity, will in general be different during each of the different ISIS frames within the superframe. If the duration time of the field is a multiple of 20ms it is possible to have one frame in the superframe mapping out the response of the sample as the field is applied and one frame ($n\times$20ms later) showing the relaxation of the sample after the field has been removed. This is illustrated in figure 4 which shows a schematic representation of a (5

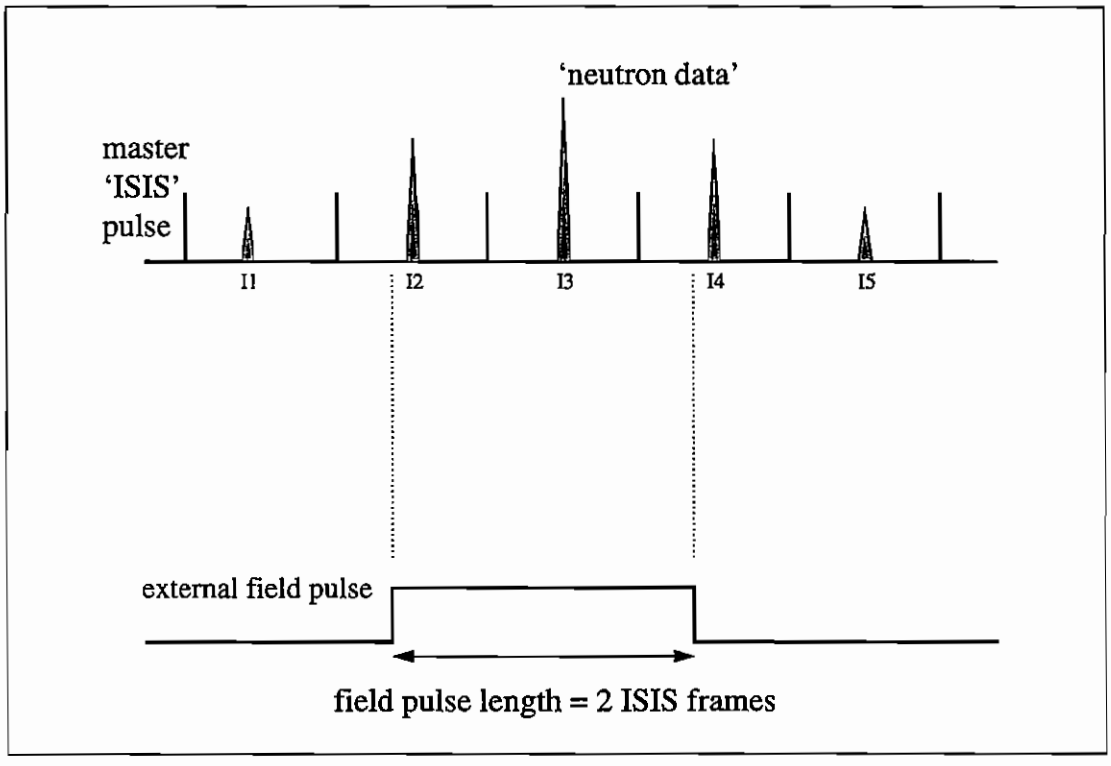

Figure 4: A schematic representation of a (5 ISIS frame) superframe in which the external field is applied before the neutrons reach the sample during the second ISIS frame. The scattering intensity I2 represents the state of the sample after a short exposure to the field. I3 is the scattering intensity after a further 20ms. I4 gives the scattering intensity a short time after the field is removed, and I5, the scattering intensity 20ms later. I1 is the scattering intensity a further 20ms after I5 and before the field is reapplied

frame) superframe. In the figure the triangular "neutron data" peaks can be taken to represent Bragg peaks for this example. The external field is shown being applied just before the neutrons reach the sample during the second ISIS frame. The intensity of the scattering, i.e. Bragg peak intensity, in this second frame is given as I2 and represents the scattering from the sample after a short exposure to the field. If the position of the

external field was shifted in time by small steps and at each step the measurement was repeated then it can be seen that I2 would map out the response of the sample as a function of real time. Since the external field length is exactly 2 ISIS frames, moving the position of the external field in small time steps to map out the response of the sample (I2) will mean that the scattering recorded in the fourth frame, I4, will show the relaxation of the sample as a function of the same real time. This is simply because the choice of duration of the field is an exact multiple of 20ms, the ISIS frame length. In other words applying the field $x\mu$s before the arrival of the neutrons in the second frame means that the field will be switched off $x\mu$s before the neutrons arrive at the sample in the fourth frame. For the rest of the superframe the intensity measured in the third ISIS frame is the scattering from the sample after a further 20ms exposure to the field from I2. The intensity in the fifth ISIS frame, I5, shows the relaxation of the sample a further 20ms from I4 and the intensity, I1, shows the state of the sample after a further 20ms from I5. Normally such a superframe would correspond to the situation where the sample had completely responded to the application of the field and then completely relaxed after the field had been removed. In the example in figure 4 the fully responded state would be I3 and the completely relaxed state would be either I1 or I5 or both.

2.3 The Superperiod Approach

The superperiod approach is used to measure properties in samples that occur over a time period of greater than 440ms, this being the maximum allowed by the superframe approach. This limitation of the superframe approach is not inherent within the TRS system but rather it is a limitation of the time channel generator (TCG) within the instruments data acquisition electronics. The TRS system is in fact capable of generating a superframe with a length of up to 65535 ISIS frames which equates to a time of (65535×20ms=) 21.8 minutes. There is however a way around this 440ms limitation set by the time channel generator which is exploited by the superperiod approach and which utilises a facility that has existed in all the ISIS DAE systems since their original design but which has never been previously used. This facility controls the way in which data is mapped onto the permanent memory in the ISIS DAE. As data comes into the DAE from the detectors it is initially stored in one of two temporary memory locations. For a normal 20ms ISIS frame this temporary memory would for example consist of 20000 time channels of width 1μs for each detector. When, following the next ISIS pulse, more data is received by the DAE this new data will be directed to the other (second) temporary memory location. While this second temporary memory is being loaded with counts, the data that was contained in the first temporary memory will be transferred to the DAE's permanent memory where it is summed with any previously stored data. Note that this transfer of data from temporary memory to permanent memory is inhibited if a veto signal is received by the DAE during the time period of the first frame. Once the second temporary memory has been loaded and another ISIS master pulse has arrived, the next set of data will now be directed to the first temporary memory location, which is now empty, and the data in the second temporary memory is now transferred to the permanent memory of the DAE. These first and second temporary memories are known as "ping-pong" memories. In the superframe approach to real time scattering the whole superframe of n ISIS frames is stored in one of the ping-pong memories before being transferred as a whole to the DAE's permanent memory. In the superperiod approach however

each ping-pong memory only contains a single 20ms ISIS frame at any one time, just as in the case of normal DAE operation. The difference between the superperiod mode of operation and the way in which the DAE normally works is to do with the transfer of the data from the temporary ping-pong memory to the permanent memory. As stated earlier, and as shown schematically in figure 3, in normal operation each 20ms ISIS frame contained in temporary memory is transferred onto (and summed with) the same single block of locations in permanent memory. In the superperiod approach this is not case since here ISIS frames are mapped onto different blocks in the permanent memory. These blocks of locations in the DAE memory are known as periods (hence the term superperiod). In figure 3 a schematic example of a superperiod is shown. In this example the first four 20ms ISIS frames of data that come in from the detectors are mapped into the same first single period (block) of memory locations and summed together. However the next four frames are mapped into a different second period which has a different address within the DAE memory system. This process is then repeated for a third and forth period and so on. Note that the data contained in each of the periods in this example is now an average over 80ms (i.e. 4 ISIS frames) of behaviour in the sample. This is a much coarser real time resolution than that offered by the superframe approach, but since the timescale of the sample relaxation is longer than 440ms then it does not matter if the resolution is coarsened in this way. Once the sample has fully relaxed the next step would be to stop collecting and storing the superperiod data and to repeat the whole measurement procedure starting with the application of the external field. The data from this second superperiod measurement would be summed together and stored in exactly the same way as for the previous measurement using the same period addresses. This will result in data from the first measurement being summed with the data obtained from the second measurement.

As noted earlier the facility for doing this mapping of frames to periods has existed in the ISIS DAE since its creation but has never been exploited before. The mechanism by which data is transferred from temporary memory to permanent memory on all ISIS instruments is as follows. First the instrument control computer downloads a 1 byte value into an 8 bit memory within the DAE which determines how many ISIS frames are to be grouped together. In the example in figure 3 this would be the number 4. Within the DAE there is also a 1024 byte memory (i.e. 256 locations by 4 bytes) which stores the values of 256 starting addresses (which lie within the range of addresses in the permanent memory). As the 20ms ISIS frames come in from the detectors the data from these frames are initially transferred from the ping-pong memory to a starting address in the permanent memory which corresponds to the value of the starting address contained in the first of the 256 locations held within the 1024 byte memory. At the same time another 8 bit counter is incremented every time an ISIS frame is received by the DAE. When this 8 bit counter reaches the value which is equal to the number of frames that are to be grouped together, it causes the (permanent) memory address to which the ISIS data is sent to be changed to the value of the starting address which is contained in the second of the 256 locations. This process will continue until all 256 locations (starting address values) have been used up. After the 256^{th} location has been used then the value of the starting address stored in the first location is once more used. It should be noted that the values of the 256 starting addresses are downloaded from the instrument control computer at the start of a run. These values do not have to be different, in fact in normal operation the 1024 byte memory contains 256 identical starting addresses which ensures

that all frames are overlapped on top of each other. Furthermore, in normal operation the value of the number of frames to periods is just one.

This ability to map frames onto different locations in permanent memory has been exploited in the superperiod approach in order to allow for the measurement of real time behaviour beyond 440ms. This was done as follows. A base unit of the number of ISIS frames that are to be grouped together is chosen. This is the F2P (frames to period array element) value which is 4 in the example shown in figure 3. Then a superperiod number, N_{SP}, is chosen such that the time $N_{SP} \times F2P \times 20ms$ is long enough for the sample to fully relax. The superperiod number is therefore the number of period array elements which must be daisy chained together. It should be noted that the value of N_{SP} is restricted to a choice of 1, 2, 4, 8, 16, 32, 64 or 128 so as to be commensurate with the 256 locations in which starting addresses can be stored. As an example, if $N_{SP} = 4$ the same set of 4 starting addresses will be stored in the 256 locations within the 1024 byte memory a total of 64 times. This means that the permanent memory address contained in location 1 within the 1024 byte memory will be the same as that in location 5, 9 and 13 and the address in location 2 will be the same as that in location 6, 10, 14 and so on for all four addresses.

The superperiod described above contains a total of $N_{SF} = N_{SP} \times F2P$ single ISIS frames which means that N_{SF} is the equivalent superframe length of the superperiod. In fact this is how the TRS system is configured for a superperiod measurement, as a superframe of length of N_{SF} frames with the delay and duration time of the external field set as for a superframe style measurement. In other words the relationship of the TRS system to the control of the external field is the same for both superframes and superperiods. The significant difference though in the behaviour of the TRS system for a superperiod measurement compared to a superframe measurement is that every ISIS master pulse is now passed to the DAE in order to cause the 8 bit F2P counter to be incremented.

2.4 The Software Approach

If a situation arose where even the superperiod approach was unable to measure the relaxation of a sample then the final time resolved technique, the software approach could be used. This approach simply involves carrying out a number of complete runs where the DAE is operating in its normal mode i.e. collecting single ISIS frames and storing them into just one period address. Before the start of the first run the external field would be applied to the sample for a time which would ensure the the sample had fully responded to the presence of the field. The field would be switched off and the first run started. The run would be programmed by the instrument control computer to last for a time of 20s upwards depending on the level of scattering that was received from the sample at the required level of statistics. At the end of the run another run would be started for the same amount of time and this procedure would continue until such a time as the sample had fully relaxed. The data collected during each run would then represent a time average of the behaviour of the sample over the time taken to carry out the run. The TRS system has very little involvement in this approach except to provide some basic control over the external field which can be switched on and off, if so desired, using commands entered via the instrument computer keyboard or by means of a command file without the requirement of superframes to activate the external field control system.

3 The Time Resolved System

In order to carry out time resolved measurements on a ferroelectric sample required the design and construction of two systems. The first is the previously described TRS system which is a logic circuit contained within a field programmable gate array (FPGA) as described in the next subsection. The programming of the FPGA was part of the work carried out for a Ph.D. thesis [2]. The TRS system is capable of performing a number of functions that include the interception of the master (ISIS) pulses from the proton pulse sensor, the generation of superframes and the production of the external field trigger signal which is used to control the second system, the high voltage switching (HVS) system. The HVS system is a set of high voltage equipment that is capable of applying up to 5kV (dc) across a single crystal sample at switching frequencies of up to 50Hz. This second system is discussed separately in section 4.

The remainder of this chapter describes the functions of the TRS system detailing how it produces both superframes and superperiods. A full schematic description of the TRS system complete with the original circuit diagrams is contained in appendix A.

3.1 The Field Programmable Gate Array, FPGA, system

The FPGA device is made up of an array of programmable logic cells that can each perform a multitude of common logic functions such as that of a simple NAND gate or a NOT element. By using combinations of cells more complex functions can be performed, such as for example those of a binary counter, a multiple input comparator or a data register. The FPGA used for this project was produced by the Xilinx company (model 4006PQ160C-5) and contains 256 individual logic cells. The programming of the FPGA was done using the Xilinx XACT software running on a Sun Sparc 10 workstation, that allows the programmer to construct the required logic circuit using standard logic symbols which are displayed on a computer screen. The actual circuit diagrams which make up the time resolved system can be found in Appendix A. Once the design has been completed the software processes the design and saves it in the from of a hexadecimal text file. The text file produced by the Xilinx software is then stored within a small EEPROM chip using a personnel computer and a programming rig. The function of the EEPROM is to feed this data out to the FPGA when both circuits are powered up. The data is used to operate sets of transistor switches that are located in each logic cell of the FPGA. It is the final state of these switches in each cell, whether closed or left open, that determines not only the functionality of that particular cell but also how it interacts with the rest of the cells within the FPGA. This process of activating the transistor switches takes about 100ns and once complete all input/output pins of the FPGA that are actually being used are put into a conducting state. These input/output pins are initially held in a high impedance state thus isolating the FPGA from the rest of the circuit board (with the exception of the one pin through the hexadecimal data is passed) until the circuit has been successfully loaded. If power is removed from the FPGA it loses the information contained within it because all of the transistor switches will default to an open circuit state and all input/output pins will be placed into a high impedance state. The FPGA will be reconfigured by the EEPROM once the power is restored.

The chosen location for the Xilinx FPGA programmed with the TRS system was the instruments DAE NPM2 board. The FPGA was positioned in the top left corner

(component side) of the board as can be seen in figure 5. The NPM2 board was chosen (a) because it offered enough space to locate the FPGA and (b) because this board also carries the ISIS (master) pulse signal which the TRS system uses to create superframes and a time delayed external field signal. On the NMP2 board the original wire carrying the ISIS pulse signal from the proton pulse sensor to the instruments DAE has been physically separated with the proton sensor end becoming one input to the FPGA and the other end of this wire now connected to one of the output lines of the TRS system as described in the next section.

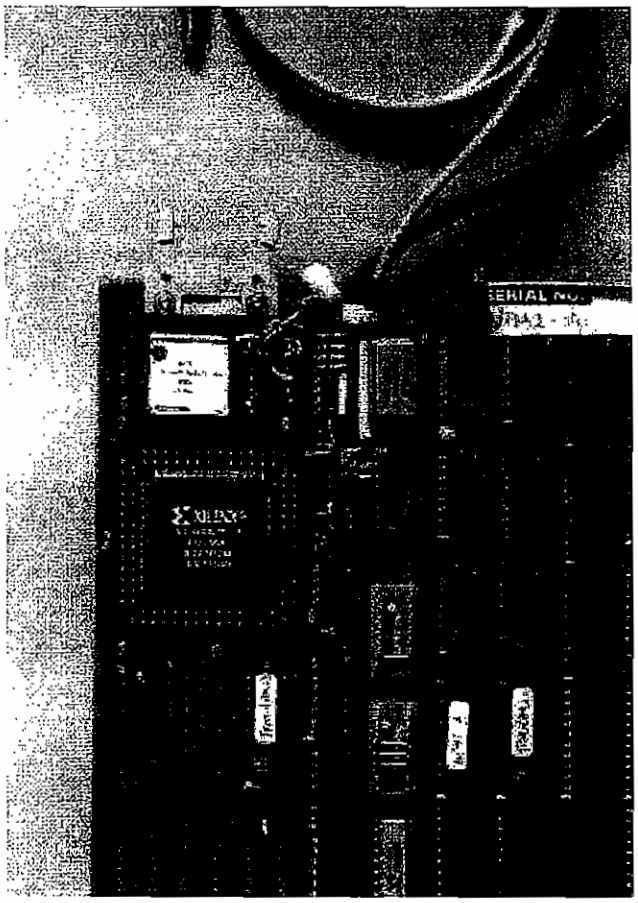

Figure 5: The Xilinx Field Programmable Gate Array (FPGA). This photograph shows the FPGA mounted onto a carrier board. Above the FPGA is a 10MHz oscillator used for timing purposes by the FPGA. Above and slightly to the right of the top right hand corner of the FPGA is the EEPROM (white strip drawn on chip) used to program the FPGA.

3.2 The Basic Functions of the TRS system

A simple block diagram of the TRS logic system giving all the main input and output signals, is shown in figure 6(a). One of the input signals to the TRS system shown in the diagram is the 50Hz ISIS pulse train from the proton pulse sensor. For time resolved measurements using the superframe approach the TRS system is required to intercept a chain of these pulses and stop them reaching the DAE so that the relevant ISIS frames

will be daisy-chained together to form a superframe. Figure 6(b) shows a schematic representation of a superframe generated by the TRS system. The TRS system produces the superframes by allowing one (arbitrary) ISIS pulse to be gated straight through to the DAE output line of the Xilinx, this pulse is represented by the first shaded 'DAE' pulse in the figure 6(b). After this pulse has been gated through, the TRS system then prevents all other ISIS pulses up to and including pulse 'n' from reaching the DAE. Following pulse n the next ISIS pulse, the second shaded pulse in figure 6(b), will be allowed to pass through the TRS system to complete the superframe. Since the DAE time of flight electronics can only be reset by those DAE pulses that are allowed through, using superframes means that the time of flight electronics will be reset less often hence allowing the DAE to collect data for longer periods of time. Exactly how the TRS logic system does this is discussed in the next section.

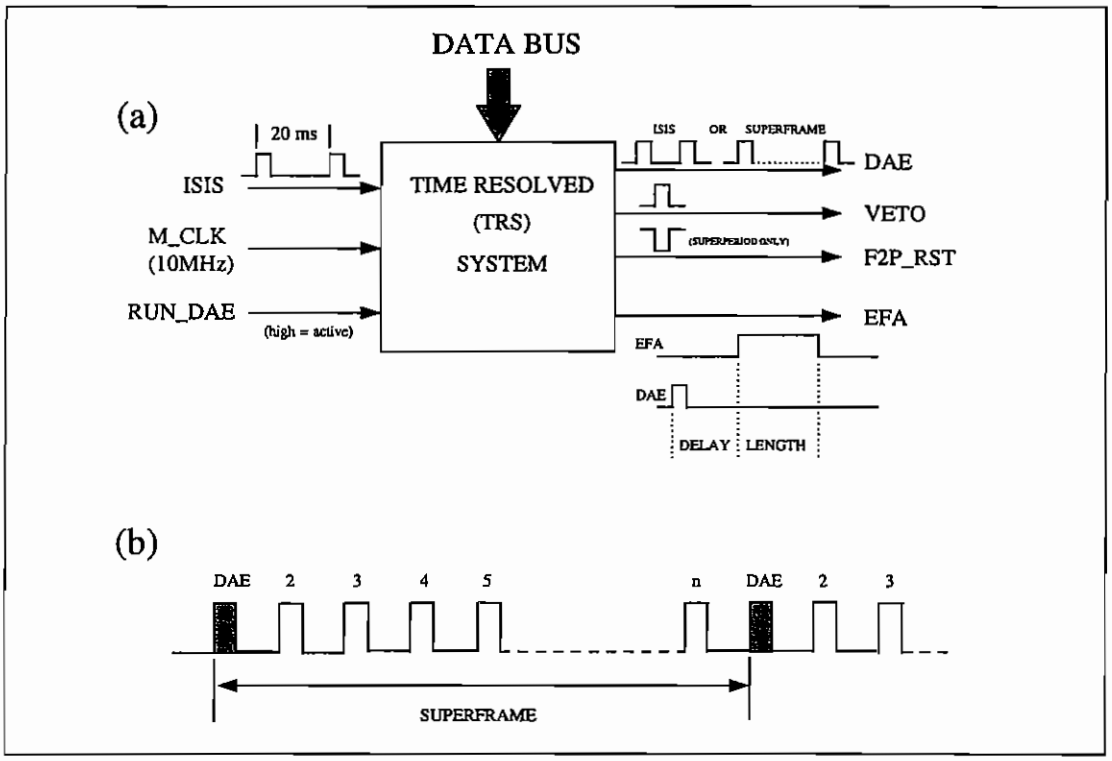

Figure 6: Part (a) shows a 'black box' description of the TRS system with all the main input and output signals. A schematic representation of a superframe is shown in part (b).

In addition to producing superframes, the TRS system also provides the External Field Activate, EFA, pulse which is used to trigger the high voltage switching (HVS) system. This system is described in section 4 which reports on the first two time resolved experiments which both used this system. Figure 6(a) shows that this EFA pulse can be delayed with respect to the signal on the DAE line. This delay can be programmed into the TRS system via the 16 bit DATA BUS which also carries information entered using the PRISMA computer regarding the required length of the superframe. The length of the EFA pulse can also be varied under software control via the DATA BUS. Details of the EFA delay and length specifications are contained in the next section. Below the DAE output line in figure 6(a) is the VETO signal line which is also wired into the

instruments DAE. If the ISIS neutron source fails when the TRS system is operating, the TRS system will produce a (90μs) positive VETO pulse which forces the DAE to reject all data contained in the current (incomplete) superframe. In effect the VETO pulse prevents the transfer of the superframe data from temporary memory to permanent memory.

The two remaining inputs to the TRS logic system are the 10MHz clock signal, M_CLK, and the RUN_DAE signal. The M_CLK clock signal is produced from a highly stable 10MHz oscillator (shown in figure 5) and is sent to the TRS system where it is used as the main timing signal as explained in the next section. The RUN_DAE line comes from the instruments DAE and is active (high) when PRISMA is running i.e. collecting data. This line is used to enable a logic circuit within the TRS system which allows the EFA signal to be fed out of the TRS system to activate the high voltage switching system. If PRISMA is not running this line will be held low which will have the effect of inhibiting the EFA signal. This is a safety feature to ensure that when the instrument is in its standby mode, which is the only time access to the sample is possible, the external field will be automatically switched off by the action of the DAE_RUN line.

Figure 7 shows how the TRS system works with the DAE during a superframe experiment. The TRS system supplies the DAE with the superframe pulses and when necessary the VETO signal if there is a problem with the synchrotron. The TRS system also supplies the high voltage switching system with the EFA trigger pulse. The high voltage system will then apply the high voltage field pulse to the sample at a time based upon the arrival time of the neutrons at the sample. All of the functions of the TRS system are software controlled by the instrument control computer and the necessary instructions are passed to the TRS system via the setup/control data highway.

The final (output) signal line in figure 6(a) is the F2P_RST line which is active only when the TRS system in running in its superperiod mode. Section 2.3 discussed how, when running in the superperiod mode, the single ISIS frames were no longer simply summed within the same memory location but instead stored in up to a maximum of 256 different locations (periods) within the DAE. This switching between memory locations is accomplished using an 8-bit counter within the DAE which must at all times be synchronised to the 'superframe' counter within the TRS system which responsible for applying the external field at the same time point in time in each superperiod. When the TRS system and the ISIS neutron source are running normally these counters will always be in synchronisation. The only time a problem can occur is when the ISIS pulsed source fails. Should this happen the superframe counter in the TRS system will automatically be reset to zero ready to begin a new superperiod. However the counter in the DAE electronics which would simply wait for the next ISIS pulse to increment the counter and would continue the superperiod from the point at the failure occurred. To avoid this problem a negative pulse is generated by the TRS system which appears on the F2P_RST line which will then reset the 8-bit counter within the DAE electronics so that is ready for the start of a new superperiod once the ISIS pulses return. Figure 8 shows how the TRS system works with the DAE during a superperiod experiment. The difference here to that shown in figure 7 is first that the ISIS signal from the TRS system to the DAE is standard 50Hz signal and not the superframes as before. Also there is now the F2P_RST signal from the TRS system to the DAE which is used to reset the 8 bit counter as described above.

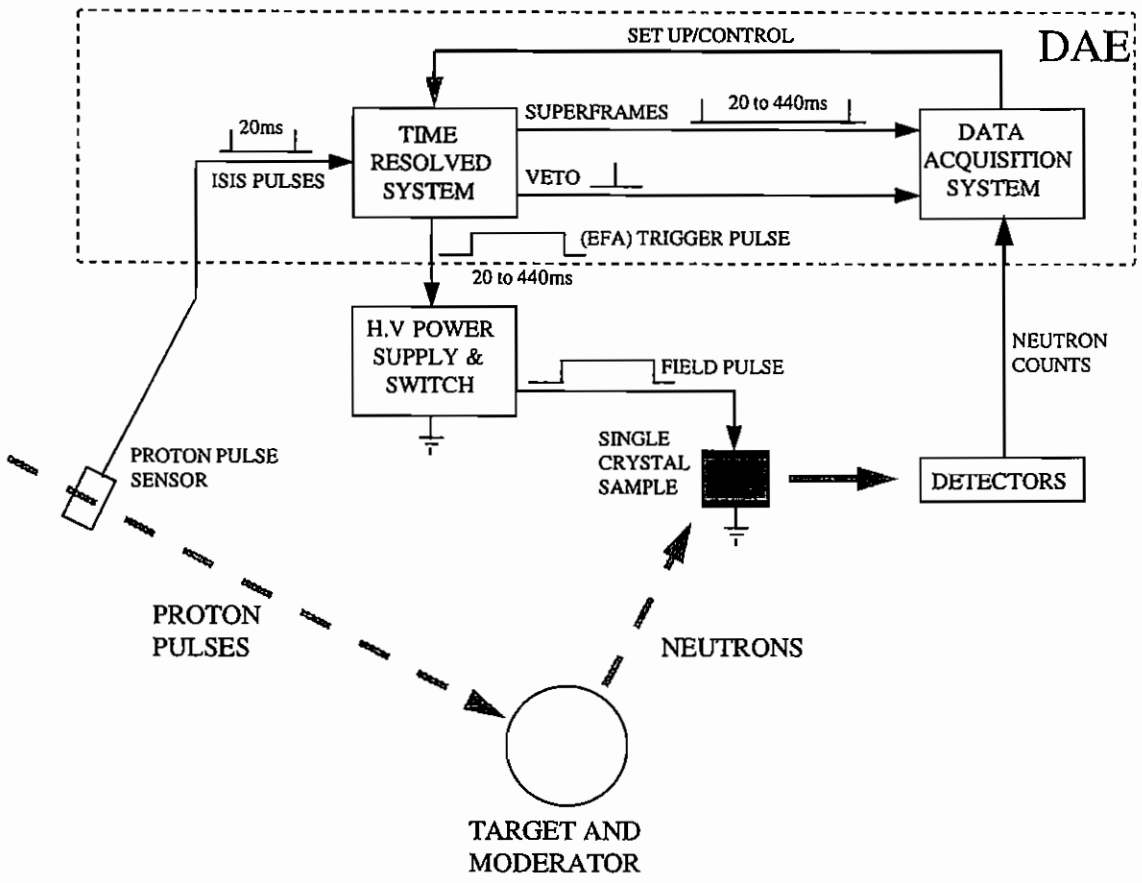

Figure 7: The DAE-TRS system set up using the superframe approach showing all the major input and output signals as described in the text.

3.3 Functional Description of TRS System - Superframes

The time resolved system is made up of 6 subsystems which are shown in block diagram format in figure 9. These subsystems are

- system and register control,
- a limit generator,
- a comparator,
- a superframe register,
- the external field control system,
- a watchdog circuit.

The process by which the TRS system produces superframes and the EFA trigger signal for the high voltage switching system will be described from the point in time after the n^{th} ISIS pulse of the superframe, as depicted in figure 6(b), has been received by the TRS system and before the next ISIS pulse (shaded pulse in figure 6(b)) is gated through as the first DAE pulse of the next superframe. At this point the TRS system is not active

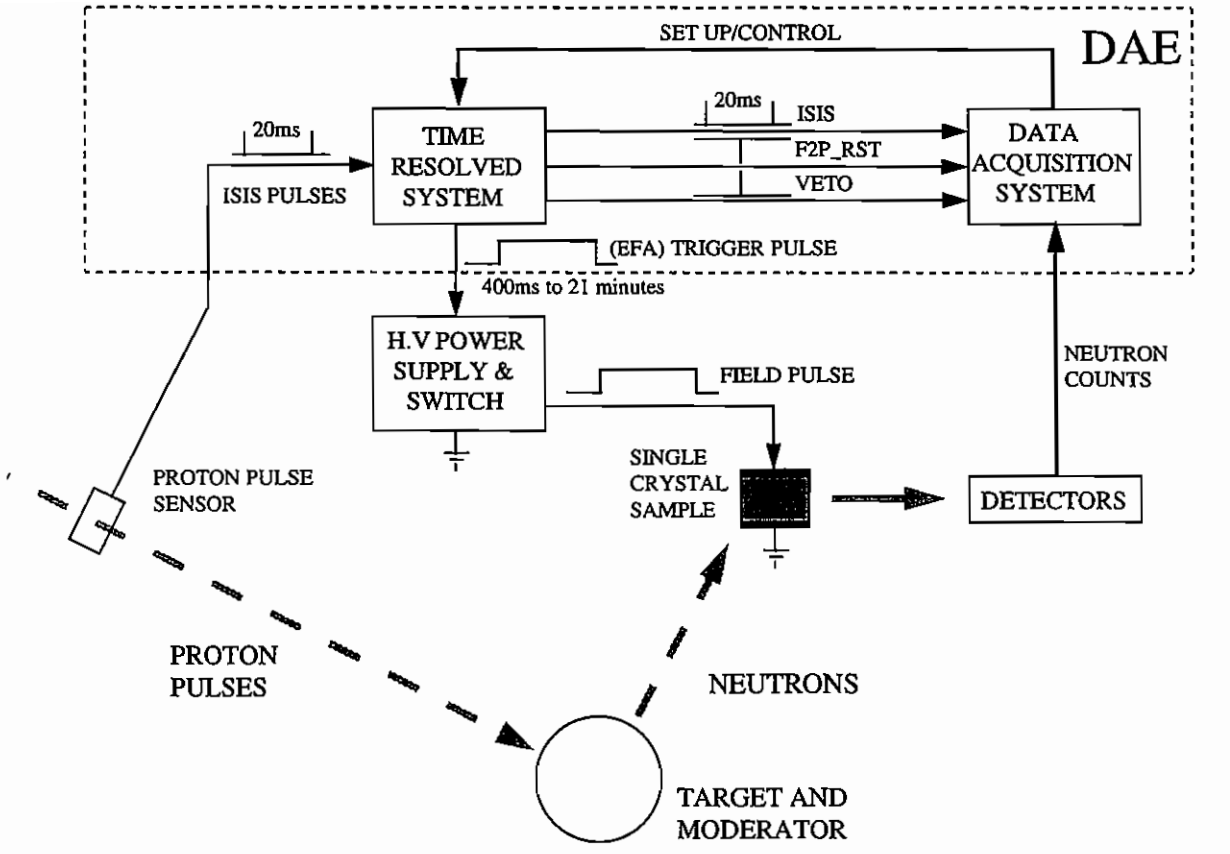

Figure 8: The DAE-TRS system set up using the superperiod approach showing all the major input and output signals as described in the text.

and the last superframe is now considered complete. The next ISIS pulse to arrive at the TRS system will be used to initiate the start of a new superframe. When the ISIS pulse arrives at the TRS system it is routed, like all ISIS pulses, to system (and register) control as shown in figure 9. Here it is immediately rerouted out again as an ISIS_INT pulse to be gated through the superframe register following the solid/dotted path in figure 9 and on to the DAE electronics via the DAE output line. The receipt of this pulse by the DAE signals the start of the superframe. This first ISIS pulse of the superframe is shown in the waveform diagram of figure 10 as pulse (a). This diagram shows all the major signals that are produced during the construction of a superframe and will be referred to frequently in the text.

When an ISIS_INT pulse is gated through the superframe register it produces a SuperFrame Count (SFC) pulse (pulse (l)) in figure 10. The job of the SFC signal is to initiate the production of the EFA trigger pulse, pulse (m), from the external field control subsystem. Once triggered the external field control subsystem will produce the EFA signal at a predetermined time from 0 to 655.35ms after the production of the SFC pulse. This delay time is programmed into the external field control subsystem in units of $10\mu s$ from the instrument computer via the 16 bit data bus. The maximum count for a 16 bit bus is 65535 which multiplied by $10\mu s$ gives a maximum delay time of 655.35ms. In addition to the delay time, the length of the EFA pulse can also be varied, again up to

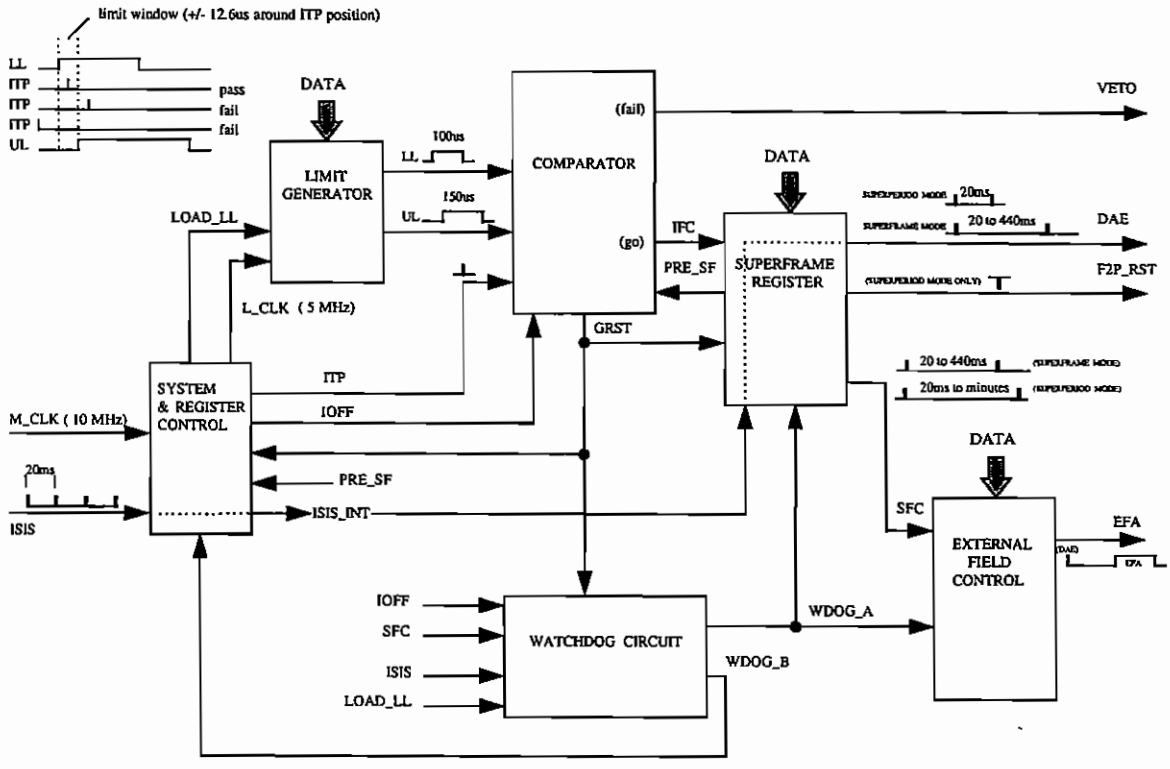

Figure 9: Schematic layout of the six subsystems that make up the TRS System showing all the main control signals.

a maximum of 655.35ms in 10μs steps. The EFA signal is fed out of the TRS system to the system which applies the field to the sample, in the experiments so far this has been a high voltage switching system (section 4) where it is used to control the application of the external field to a sample.

The first ISIS pulse of the superframe is also gated out of system control to one of the three inputs of the comparator subsystem (see figure 9) as the relabelled ISIS Timing Pulse (ITP) signal. The job of the first ITP pulse of the superframe is to activate the comparator subsystem in preparation for all subsequent ITP (i.e. ISIS) pulses. The first ISIS pulse received also enables the 5MHz clock signal, L_CLK, within system control which subsequently activates the limit generator. The limit generator subsystem uses the 5MHz clock signal to produce two separate pulsed signals, both of 50Hz, one consisting of the Lower Limit (LL) pulses of 100μs duration and the other consisting of the slightly longer Upper Limit pulses (UL) of 150μs duration. The two pulse trains will not however appear until ~20ms after the L_CLK line has first become active for the reasons described later. With the comparator and the limit generator enabled the TRS system waits for the next ISIS pulse which will be pulse (b) in figure 10. Just before the nominal arrival time of the ISIS pulse (b), which will be ~20ms after ISIS pulse (a), the first of the 100μs LL pulses (pulse (c)) will be produced from the limit generator. These LL pulses are directed to a second input of the comparator circuit as shown in figure 9. The actual

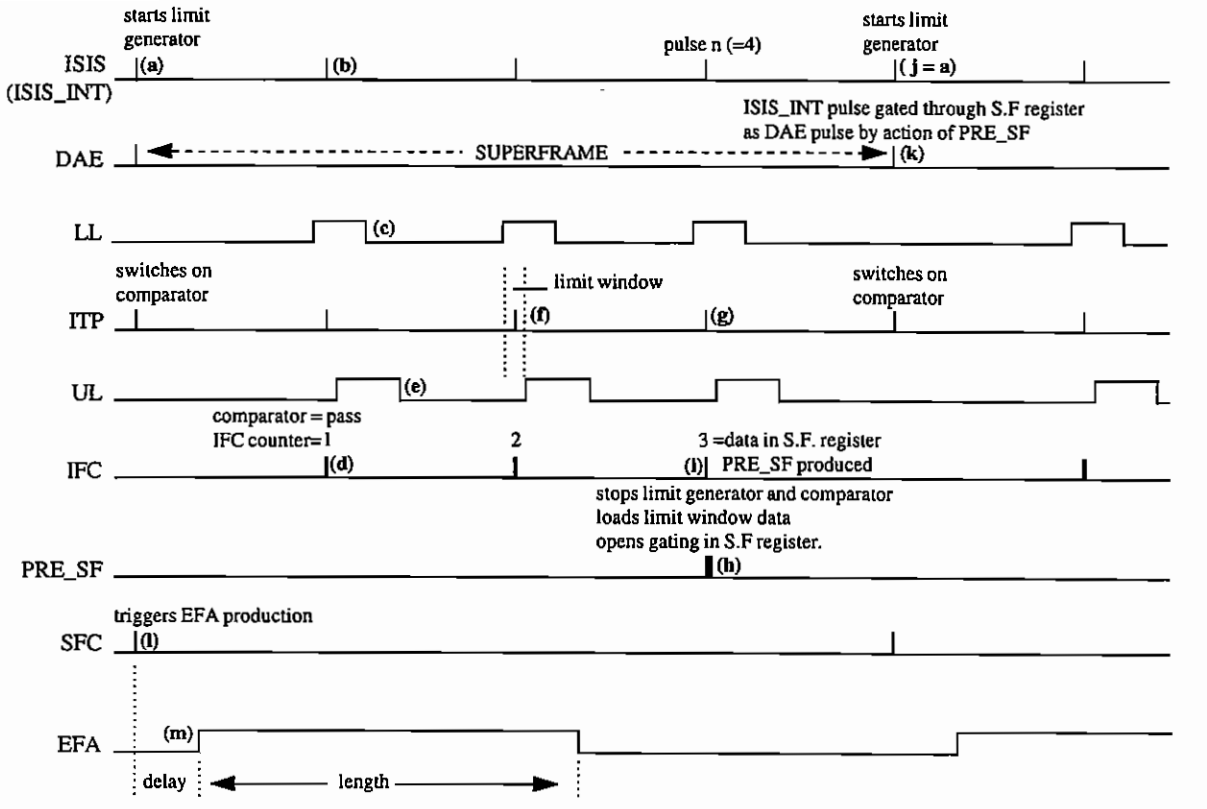

Figure 10: A waveform description of the operation of the TRS system in the superframe mode. See text.

timing of the LL pulse is controlled by the limit generator which is programmed to allow the LL pulse to appear at a certain time interval up to a maximum of 12.6μs before the expected arrival time of the ISIS pulse at the comparator. As already stated the limit generator was initiated by ISIS pulse (a) and so the appearance of the first LL pulse is timed from that event. On receipt of the ISIS pulse (b), system control will reroute it to the comparator as another ITP pulse. Under the conditions that the LL signal is active (high), the ITP pulse is now present and the UL pulse has not yet been produced, the comparator produces a 'pass' signal in the form of a ($\sim$170μs) ISIS Frame Count (IFC) pulse - pulse (d) in figure 10. At a predetermined time (up to 25.2μs as programmed by the instrument computer) following the appearance of the first LL pulse the first UL pulse, pulse (e) will be produced by the limit generator. If for some reason an ITP pulse fails to reach the comparator before the UL pulse, a VETO (ie. 'fail') signal would be issued by the comparator and sent to the DAE electronics which would result in the rejection of any data within the current superframe. This situation is described fully in section 3.3.1. The LL and UL pulses therefore form a 'limit window' which is shown schematically at the top left of figure 9 and also in figure 10 (ITP pulse (f) shows a 'pass' situation). The use of the limit window ensures that if the stability of the ISIS pulse source is compromised then the TRS system will reject the current data (via the VETO signal), and all further data, until such time that the stability of the ISIS source is once again restored.

The production of the two limit pulses continues up to pulse (n) of the superframe allowing the timing of each ITP pulse within the current superframe to be constantly compared to that of the UL and LL pulses. Assuming that all ITP pulses pass the limit checks then a succession of IFC pulses will be produced by the comparator and sent to the superframe register. The superframe registers task is to count these IFC pulses and compare this count against a value which has been programmed into the superframe register (via the data bus). This stored value is the length of the required superframe as measured in numbers of ISIS frames, less one. In the example in figure 10 the data stored in the superframe register would be 3 decimal since the superframe contains 4 ISIS frames. When the last ITP pulse of the superframe (pulse (g) - fig 10) has been passed by the comparator, the resulting IFC pulse (pulse (i)) produces within the superframe register a Pre-Superframe (PRE_SF) pulse indicating that the value in the IFC counter now equals the value of the data programmed into the superframe register. This PRE_SF pulse (pulse h) is responsible for the following. First (figure 9) it is sent to system control to switch off the 5MHz clock signal (L_CLK) to the limit generator thereby halting the production of the LL and UL pulses. Secondly the PRE_SF signal is sent to the comparator to disable it since the limit pulse production for the current superframe has now ceased and therefore the comparator is no longer required.

Up to now all ISIS_INT pulses have been sent to the superframe register. With the exception of the first, these pulses were prevented from passing through to the DAE output line of the FPGA, by logic gating within the superframe register that was activated when the first ISIS_INT pulse was gated through. The PRE_SF pulse disables this logic gating thereby allowing the next ISIS_INT pulse (pulse (j), in figure 10, which is the equivalent of (a)) to be gated through the superframe register as a DAE pulse (pulse (k)) signaling the end of one superframe and the start of the next.

The reason the limit generator and comparator are switched on and off each superframe is to ensure that the synchronisation between the 50Hz LL and UL pulses from the limit generator and the ISIS (50Hz) signal is always true. If the limit generator was kept running it would quickly become out of synchronisation with the ISIS clock frequency. This means that the limit window set up by the LL and UL pulses would drift in time with respect to the ISIS pulses and within $\sim$ 5s the error would be so large that it would be impossible for an ISIS pulse to appear within the limit window. The fact that the limit generator is switched off at the n^{th} pulse of the superframe means that there is no limit window to check the position of the first ISIS pulse of the next superframe. This however is not that important since it is only the timing of the ISIS pulses within the superframe that is important, the first pulse just defines the start of the superframe.

3.3.1 Possible Failures during Superframe Production

There are two reasons why the TRS system may be unable to construct a superframe. The first reason is that one of the ITP pulses of the superframe arrived outside the limit window set up by the LL and UL pulses as a result of the synchrotron frequency drifting and this situation will be dealt with first. The other reason is that the ISIS pulse was absent altogether due to a problem with the synchrotron and this situation will be considered second.

If an ITP pulse fails to appear within the limit window set up by the LL and UL pulses, the comparator will produce a VETO signal which is sent to the DAE electronics

to reject the data collected during that (so far incomplete) superframe. In the waveform diagram of figure 11, the ISIS pulse (a) is shown arriving earlier than the LL pulse and this results in the VETO (pulse (b)) signal from the comparator. There is now no point in continuing with the production of the current superframe so the TRS system is reset. To do this the comparator produces a 90μs General Reset (GRST) pulse (pulse (c)) at the same time as the VETO pulse, and this GRST pulse resets system control switching off the 5MHz L_CLK signal and thereby stops the production of the limit pulses. Further, this GRST pulse is sent to the superframe register where it resets the superframe counter to zero, and it is also sent to the watchdog circuit where it drives the WDOG_A signal high (pulse (d)). This WDOG_A signal is directed to the external field control subsystem to kill the EFA signal which is shown ending early by the dotted line on the EFA pulse (pulse (e)). The loss of the EFA signal will have the effect of deactivating the HVS system. Further SFC pulses will be prevented from triggering the external field control circuit while the WDOG_A signal is active (high). Finally, the WDOG_A signal is sent to the superframe register which will inhibit the production of further DAE pulses, again while the WDOG_A signal is high.

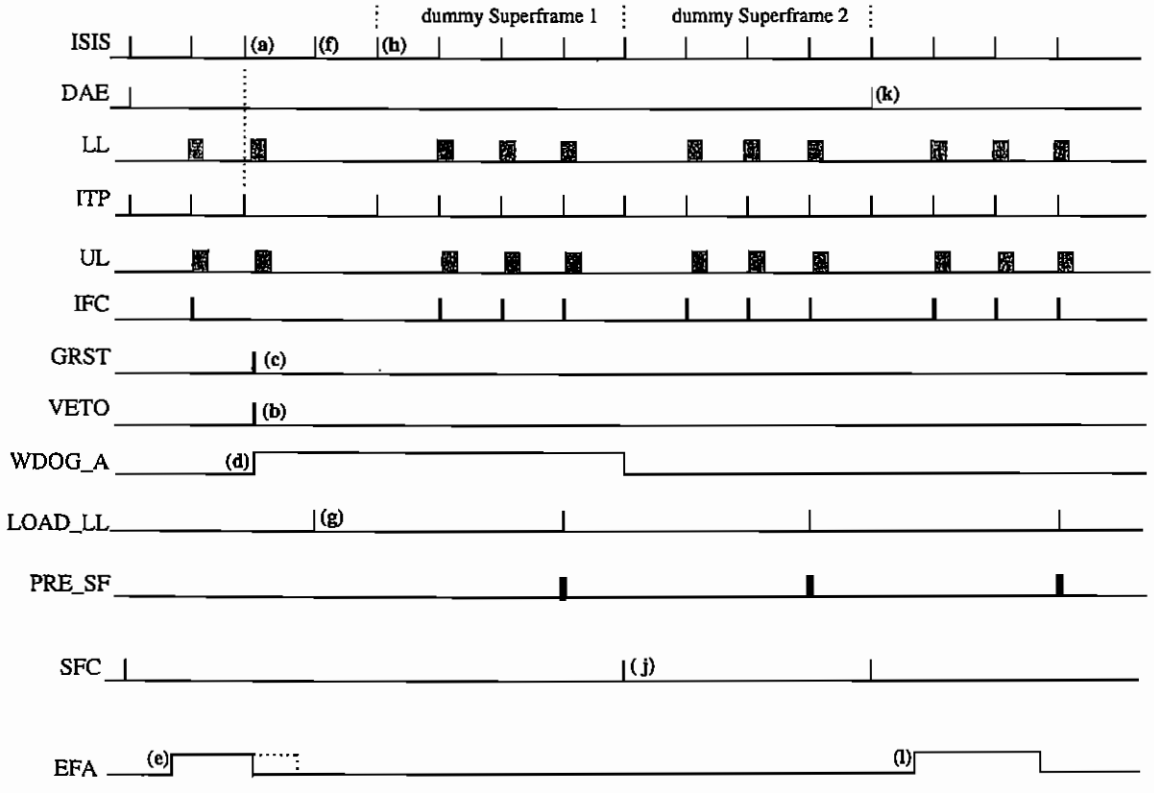

Figure 11: A waveform diagram of the major control signals that result from an error in the timing of the ISIS pulses.

With system control reset, the production of further DAE pulses inhibited, and the external field control circuit disabled, the TRS system will now await the next ISIS pulse (pulse (f)). When this happens ISIS pulse (f) will reactivate system control which in turn

will produce the LOAD_LL signal (pulse (g)) to pre-load the limit generator with the LL and UL position data stored in its data register. The next ISIS pulse (figure 11 pulse (h)) starts the limit generator by enabling the L_CLK signal and produces the first ITP pulse which switches on the comparator. This sequence starts the production of the first of two 'dummy' superframes shown in figure 11. If the first superframe is produced correctly then an SFC signal (pulse (j)) is produced which is sent to the watchdog circuit to release the WDOG_A signal. The completion of the second dummy superframe then gives rise to a DAE pulse (pulse (k)) and a SFC pulse marking the start of a proper superframe. The SFC pulse will be sent to the external field control system to produce the EFA pulse (l). If the TRS system fails to complete one of the dummy superframes it goes into a loop and will keep trying until such a time as two consecutive dummy superframes can be completed or a total failure of the synchrotron occurs resulting in the total loss of the ISIS pulse train.

A complete synchrotron failure will result in the loss of the 50Hz ISIS pulse train to the TRS system. This could happen in the middle of the superframe production when the limit generator is operational or at the end of the superframe when the PRE_SF pulse has been produced and the limit generator has been switched off. Initially the case where the limit generator is in operation will be considered. When the ISIS pulses fail the first thing that will occur will be the production of the GRST and VETO pulses from the comparator, see waveform diagram in figure 12. This happens because the UL pulse will have been received by the comparator before the (now absent) ITP (ISIS) pulse and it is this combination of an active LL and UL pulse and no received ITP pulse that results in the production of the GRST and VETO pulses. The GRST pulse is sent to the watchdog system to produce the WDOG_A signal as described in the previous section stopping the production of the superframes and the EFA signal. At a time of 10ms after the production of the WDOG_A signal the watchdog circuit will produce the WDOG_B signal. This is achieved by a timer in system control that upon reaching 30ms as measured from the last received ISIS pulse, will initiate the ISIS Off (IOFF) signal. This IOFF signal is fed to the watchdog circuit to drive the WDOG_B signal line high (pulse (a)). Normally the timer in system control fails to reach 30ms because the ISIS pulses are used to reset the timer every 20ms. If the timer is not reset before a count of 30ms is reached then the TRS system will automatically assume that the synchrotron has failed.

The WDOG_B signal is sent to system control where it inhibits the production of further ITP pulses so that no further superframes are possible while this signal is high. Also the L_CLK signal is inhibited so that production of the LL and UL pulses cannot take place. Within the watchdog circuit the WDOG_B signal enables an internal counter that is clocked by the ISIS pulses. This counter will remain at zero, and the TRS system will remain inactive with the WDOG_A and WDOG_B signals high until the neutron source is fully operational and the ISIS pulses return. When the synchrotron is running again the ISIS pulses are once more fed into and out of system control. They do nothing within system control (e.g no L_CLK signal is produced) because of the presence of the WDOG_B signal. The ISIS pulses are instead routed to the watchdog circuit to increment the internal counter that was enabled by the WDOG_B signal. Once the counter reaches 10 decimal (in 10×20ms=200ms) the WDOG_B signal will be removed. This procedure using the WDOG_B signal checks that the synchrotron is functioning normally over a 200ms period before superframe production recommences. If the ISIS pulses are lost again before the end of the 10^{th} pulse counting period then the counter will be reset back

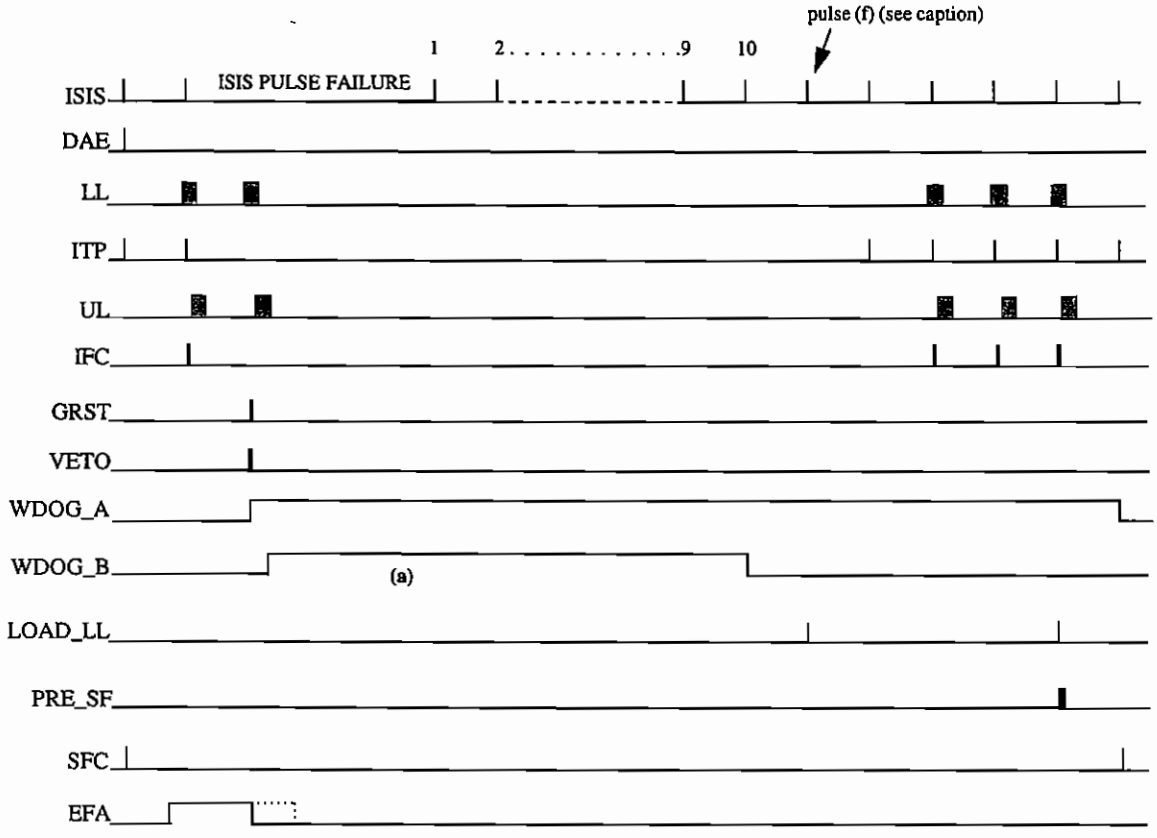

Figure 12: A waveform diagram of the major control signals for the case of a complete synchrotron failure. ISIS pulse (f) in this diagram is the equivalent of ISIS pulse (f) in figure 11.

to zero by the resulting IOFF signal. When the WDOG_B signal is released the TRS system is in the same state as it was following a reset caused by a positioning error of an ISIS pulse within a superframe as described in the previous section ie the WDOG_A signal is active high. The start up procedure from this point is the same as described before i.e. starting off with the 2 dummy superframes.

Finally, if the synchrotron fails at the end of the superframe when the limit generator has been switched off the the action of the circuit is slightly different. This time the GRST and VETO signals will not be produced at this stage since the comparator and limit generator system are not being used. The IOFF signal will however be produced at the 30ms point following the last ISIS pulse and this IOFF signal is sent to the comparator to produce the GRST pulse. The operation is then the same as described above.

3.4 Functional Description of TRS System - Superperiods

The operation of the TRS system in the superperiod mode is essentially the same as for the superframe mode with only a few small differences which are discussed in this section. The first difference is that the limit generator subsystem and some of the comparator functions are not used in the superperiod mode. In figure 9 this means that the LL and

UL pulses from the limit generator to the comparator are not produced, the LOAD_LL and L_CLK pulses to the limit generator are inhibited as is the ITP pulse from the system and register control to the comparator subsystem. If the limit generator and comparator were used in the superperiod mode to monitor the periodic time of the ISIS pulses, the synchronisation between the master ISIS "clock" pulses and the 50Hz clock in the limit generator would be lost within ~5s from the start of the superperiod causing a reset condition within the TRS system. Therefore superperiods of greater than 5s duration would not be possible.

Switching off the limit generator and comparator will allow the natural wandering of the ISIS frequency to go unchecked. In the case of the superframe where this wandering becomes excessive a blurring of the real time resolution would occur since the position of the ISIS frames within the superframe would become shifted in time with respect the external field pulse which is fixed in time from the first, T=0, ISIS pulse of the superframe. The use of the limit generator and comparator subsystems in the superframe mode restricts this blurring of the real time resolution by setting a maximum limit that will be accepted for any changes in the periodic time of the ISIS pulses thereby ensuring that this effect is small compared to the time scale of the behaviour that is being measured in the sample. For the case of a superperiod experiment the time scale of the changes occurring within the sample is now so much longer that any slight blurring of the real time resolution is of no significance.

Another way in which the TRS system operates differently in the superperiod mode is that now all the ISIS pulses are sent directly out to the DAE electronics via the system and register control circuit and the superframe register circuit as shown by the solid/dotted path in figure 9. There is now no interception of these pulses like there is in the superframe mode. The superframe register does however still daisy chain ISIS frames together to form superframes which as for the superframe mode are used to trigger the external field control circuit using the SFC pulse. The external field control circuit operates in exactly the same way for the two modes of operation.

The watchdog circuit also operates in the same way in the superperiod mode as it does in the superframe mode working with the GRST pulse to switch off the TRS system if the ISIS neutron source should fail as described in section 3.3.1. Although the comparator no longer checks the frequency of the ISIS pulses it still monitors the IOFF signal line which will become active if the ISIS synchrotron should fail. In this situation the F2P_RST output line from the comparator subsystem, see figures 8 and 9, becomes active producing a negative going pulse (an inverted GRST pulse) which is used to reset the 8-bit period counter within the DAE electronics. This ensures that the period counter in the DAE and the IFC (superframe) counter in the superframe register are always synchronised to each other. Under normal running they are incremented by the same ISIS pulse and so this is always true but in the event of an ISIS failure only the IFC counter is automatically reset. The TRS system has to ensure that the period counter is also reset and it does this by producing the F2P_RST pulse.

4 The High Voltage Switch System

The time resolved technique described in this thesis was initially developed to investigate phase transitions in ferroelectric materials and therefore a high voltage switching (HVS) system was constructed as part of this project to provide the necessary pulsed electric fields to the sample. The HVS system is a collection of several pieces of high voltage equipment which are shown schematically in figure 13. The system consists of the following

- a high voltage push-pull switching device,
- a high voltage power supply.
- a high power resistance box,
- a TTL signal conditioning unit - the EFA signal box,
- a high voltage probe assembly and oscilloscope,

Figure 14 shows a photograph of this equipment illustrating how it is arranged. The resistance box with the (black) GHTS-100 high voltage switch sitting on top of it are situated in the centre top of the photograph. The centre output of the GHTS-100 is shown connected to the high voltage probe assembly (top left) which is in turn connected to a SHV connector, shown attached to a T-piece from a CCR. Middle bottom is the EFA signal box which is connected to the control input of the GHTS-100. The free cable at the other end of this box is connected to the PRISMA patch panel. On the right hand side of the photograph is a 10kV power supply and a cable adaptor box which allows the 10kV supply to be connected to the resistance box. Subsections 4.1 to 4.4 describe these components in more detail.

The input to the HVS system (figure 13) is the EFA signal which comes from the TRS system via a connection in the PRISMA patch panel assembly. There are two patch panels on the PRISMA beamline and these are placed approximately 50m apart and connected together by a system of multicore cables. One patch panel is situated near the PRISMA spectrometer where the HVS system is located and the other is in the PRISMA cabin which houses the instrument computer, the DAE and the TRS system. These patch panels are normally used to pass signals from the temperature sensors in the sample environment equipment used at ISIS, to the instrument computer in the PRISMA cabin. The EFA signal is of a TTL type (0-5 volt) with a pulse duration ranging from 10μs of up to 655 milliseconds, and this signal is used to control the switching of the GHTS-100 high voltage switch assembly.

The diagram in figure 13 shows a high voltage power supply, which is connected to the 'H' input of the resistance box. Inside the resistance box between the 'H' input and the output 'L' there is a series of resistors which are designed to limit the current that can be drawn from the supply when the high voltage is applied to the sample. Since the sample acts as a capacitor it will initially appear as a low impedance load to the fast rising voltage level which is being applied across it. This can result in a high current surge from the power supply causing the power supply to automatically switch off. This happens because a circuit within the power supply constantly monitors the current that is being drawn by the load it is supplying (the TGS sample in this case) and will immediately switch off the supply if a current overload situation occurs. The resistors inside the resistance box

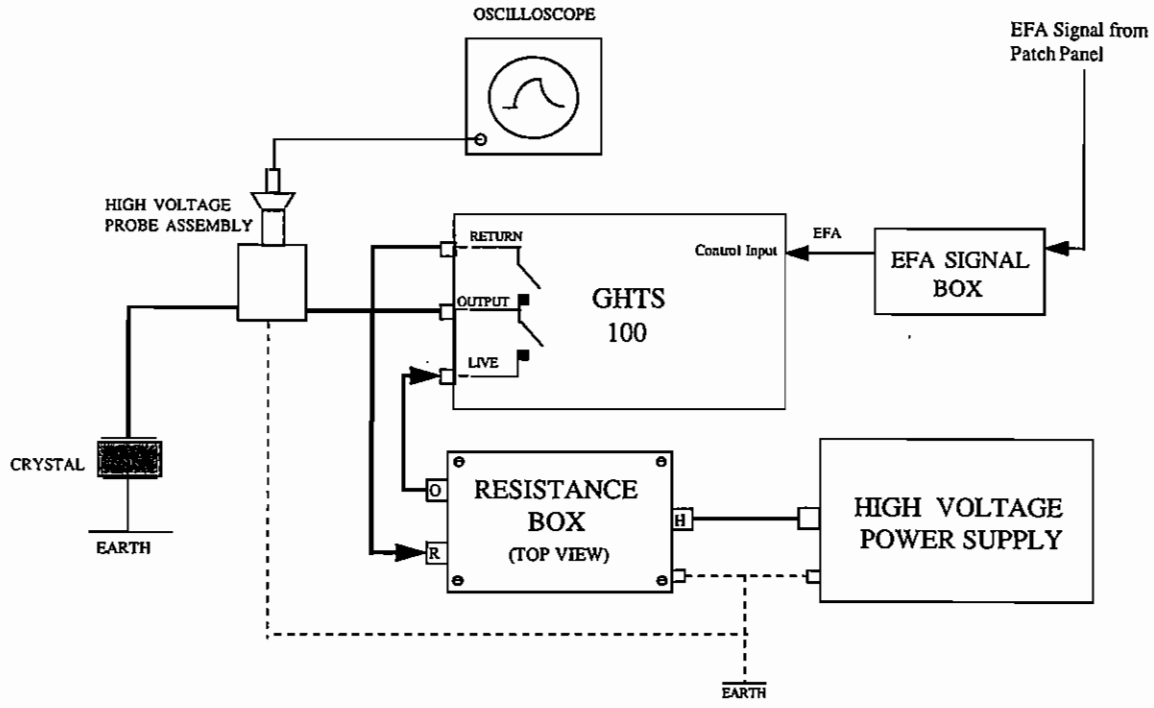

Figure 13: A schematic representation of the high voltage switching (HVS) system showing all the main assemblies.

ensure that the charging current to the sample does not exceed the rated maximum for the power supply.

The high voltage output from the power supply will, via these resistors, be present on the LIVE input of the GHTS-100 switch. When the EFA signal goes high the contact between the LIVE input and the OUTPUT connection will close, placing the high voltage directly across the sample via the high voltage probe assembly. The other contact, between the OUTPUT and RETURN connections, will remain open. These two contacts always adopt an opposite status, never being closed at the same time. The contact between the LIVE and OUTPUT connections will stay closed for the full duration of the EFA pulse. A display of the charge/discharge cycle of the electric field across the sample can be seen on an oscilloscope using the high voltage probe assembly. The output lead from the high voltage probe assembly connects directly to a special SHV socket on the centrestick of the sample environment being used. The back end of this SHV socket is connected to one of the electrodes on the sample.

At the end of the EFA pulse, the resulting low on the EFA line causes the contact between the LIVE and OUTPUT connections to open and the contact between the RETURN and OUTPUT connectors of the GHTS-100 to close. This action discharges the high voltage on the sample through the GHTS-100 and into the resistance box via the input 'R' which is then sent to an earthing point on the casing of the resistance box via

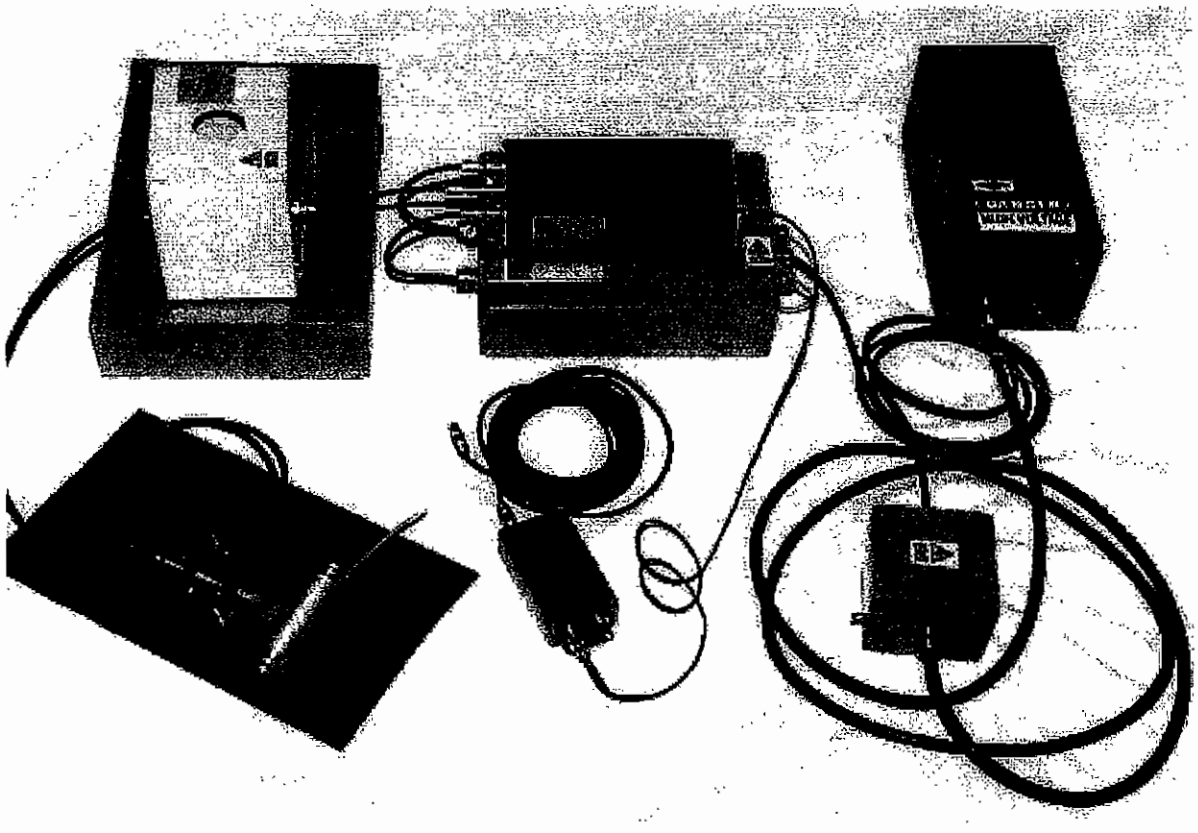

Figure 14: The layout of the HVS system. The resistance box with the (black) GHTS-100 high voltage switch sitting on top of it are situated in the centre top of the photograph. The (centre) output of the GHTS-100 is shown connected to the high voltage probe assembly (top left) which is in turn connected to a SHV connector, shown attached to a T-piece from a CCR. Middle bottom is the EFA signal box shown connected to the (control) input of the GHTS-100. The free cable at the other end of this box is connected to the PRISMA patch panel. On the RHS of the photograph is a 10kV power supply and a cable adaptor box which allows the 10kV supply to be connected to the resistance box.

another set of resistors. The total resistance of this second set of resistors is normally equal in value to the first set which allows the sample to be discharged at the same rate as it was initially charged up. Alternatively, this second set of resistors can be bypassed and the voltage on the sample can then instead be discharged via a shorting wire directly to earth, producing very fast discharge rates. Shorting the voltage across the sample to earth is not a problem if the energy stored across the sample is small. This technique of shorting the high voltage return path was used for this study of TGS. The typical capacitance of the TGS sample was found to be in the order of 1000pF. Since the energy stored in a capacitor is given as E= $\frac{1}{2}$CV^2 then using a voltage of 3000V (as was done in the TGS experiment) means that the energy stored by the sample is ~0.5 millijoules, which can easily be absorbed by the high voltage equipment.

4.1 The GHTS-100 High Voltage Switch

The heart of the high voltage switching system is the GHTS 100 push-pull switching unit from the Behlke Electronics Company, Germany. The GHTS-100 is a universal high voltage switching device designed for capacitive and resistive loads. It is triggered via its control input connection using a TTL type input (the type supplied from the EFA signal box) and when used in combination with an external high voltage supply can generate positive or negative pulses with amplitudes up to 10kV or bipolar pulses with amplitudes of up to 5000 Volts. The maximum continuous switching rate of this device is 30kHz with a maximum short burst frequency of 3MHz. The maximum power dissipation of the device is 20W (continuous) which for a purely capacitive load is calculated using

$$\text{max power} = \frac{\text{CV}^2 f}{2} \tag{5}$$

where C is the capacitance of the sample, f is the frequency of the EFA pulse train, and V the voltage across the crystal.

4.2 High Power Resistance Box

The job of the high power resistance box is to limit the initial current surge that occurs when the high voltage is first applied to the (capacitive) sample. Most modern power supplies contain a trip circuit that will activate if the circuit it is supplying tries to draw an amount of current that exceeds its design maximum. It is possible that when initially charging a capacitive load that the current surge would cause the trip circuit in the power supply to activate. The high power resistance box is designed to prevent this problem. The resistance box contains two insulating boards, placed one above the other on to which are mounted 44×2 watt carbon film resistors. A typical example of one of these boards is shown in figure 15 which shows a system of 44 × 333kΩ connected in series. This board was designed to limit the current drawn from a standard 1kV/75mA power supply. The total resistance of the 44 resistors is designed to optimise the rise time of the voltage across the sample when using certain power supplies by allowing ~ 95% of the maximum allowable current to be drawn from the power supply during the initial surge when the voltage is first applied to the sample. The rise time τ of the voltage across the sample is calculated using τ = CR where C is the capacitance of the sample and R is the total resistance of the series resistors plus the cables carrying the voltage to the sample. To

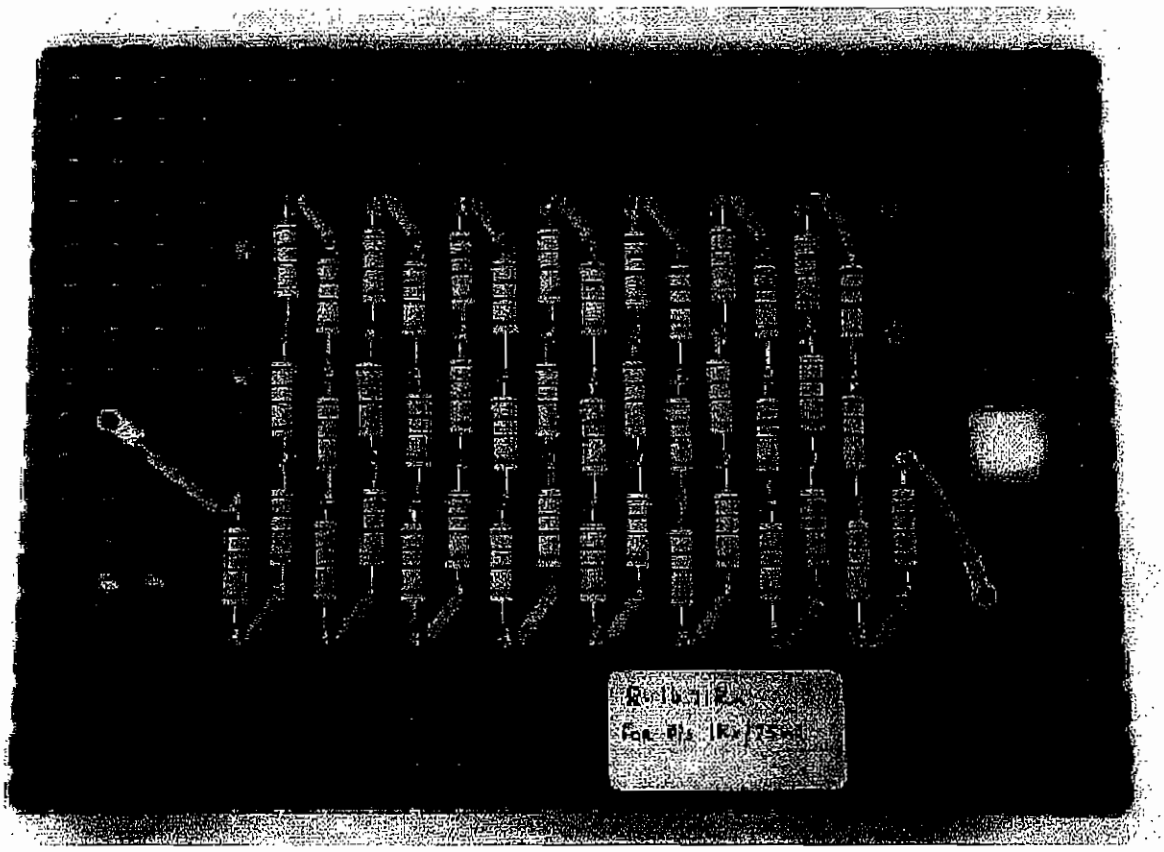

Figure 15: A typical resistor board. This board was constructed using 44 $\times 333 k\Omega$ resistors and was designed to be used with a 1kV/75mA power supply.

keep τ to a minimum R must be kept as low as possible although not so low that the current drawn from the power supply exceeds its maximum. There are two other pairs of resistor boards which are optimised for a 3kV 25mA supply and a 10kV 7.5mA supply.

The resistors on the upper of the insulating boards form part of the high voltage path between the power supply and the sample and they are internally connected between the 'H' input and the 'L' output of the resistance box as labelled in figure 13. The resistors on the lower board are the part of return path from the sample to earth and they are internally connected between the 'R' output and earth.

4.3 The EFA Signal Box

The 5V (TTL) EFA pulsed signal from the TRS system is amplified by a separate circuit on the DAE NMP2 circuit board to 15V before it is sent to the GHTS-100 high voltage switch. The EFA signal box is used to convert the EFA trigger signal back to 5V once its arrives at the PRISMA beamline. This amplification of the EFA signal is done because of the noise levels that are present in the $\sim$ 50m of cabling between the TRS system in the PRISMA cabin and the GHTS-100 switch which is located on the PRISMA beamline. Amplifying the EFA signal to 15V therefore prevents it from becoming lost amongst the background noise.

Once the EFA signal has been converted back to 5V it is boosted by a power transistor so that the signal is then capable of driving the low impedance control input of the GHTS-100 high voltage switch.

4.4 High Voltage Probe Assembly

When measuring the response or relaxation of a sample during a time resolved experiment it is important that the switching rates of the external field are much faster than those of the sample i.e. the sample is not merely just following the changing field. One way of determining if this is the case is by attaching a high voltage probe to the high voltage coax cable that connects the GHTS-100 high voltage switch to the sample. This high voltage probe can then be plugged into an oscilloscope which will then display the rise and fall times of the electric field.

To achieve the above a high voltage probe assembly was constructed which consists of a grey insulating housing which has a hole cut in its lid into which a standard high voltage probe can be inserted. The diameter of the hole was designed to take a Tektronics type high voltage probe. The input and output leads of the probe assembly connect the sample to the output of the GHTS-100 and these leads are soldered together inside the insulated housing. The point at which the leads are soldered is left exposed to allow the tip of the high voltage probe to make a clean electrical contact with the wire.

5 Software for using the TRS

There are two aspects to running the TRS in which software plays an important role. One is the software that is included within the PRISMA beamline operating program which allows the real time measurements to be set up and the other is the analysis programmes that run within GENIE which allow the data taken in such experiments to be processed. There is in fact also a third set of programmes, which run independently of the PRISMA program and GENIE which were written for diagnostic purposes. In the following sections we'll deal first with the operating system "software", which might be better described as the parameter names and values in the PRISMA program. For the superperiod mode it is also necessary to create a HARDPERIODS.DAT file which defines the structure of the periods in the DAE. This is described in section(5.7). Then after that we'll describe the data analysis software input and output and then finally the diagnostic programs. Source code listings for the various programs and macros are given in appendix B.

5.1 The TRS Parameters in the PRISMA Program

The program for running the PRISMA spectrometer has been described in *The PRISMA Operating Program Manual* [3]. The philosophy of this program, as described in ref. [3], is that certain sets of parameters form groups or families, each related to a certain aspect of the spectrometer control. These families have short names, such as SAMP (for sample parameters), TOF (for time of flight parameters), etc. and not unsurprisingly the parameters for controlling the TRS system are part of a group/family called TRS. Thus just as one can type PRINT SAMP or PRINT TOF to list the parameters and values for the sample and time of flight so one can also do **PRINT TRS** and list the parameters for the TRS system. The parameters themselves are as follows

- **EON** — This sets which *mode* the TRS system works in.
- **DELAY** — This sets the *delay* time in microseconds.
- **DURAT** — This sets the *duration* time for which the external field is applied, i.e. the amount of time it is turned on for. Again it is given in microseconds.
- **SFRAM** — This sets the *number of ISIS frames which make up a superframe.* Note the value SFRAM=1 does have to be treated in a special way, see notes later on.
- **LWIN** and **UWIN** — These two values set *window limits* for the timing of the ISIS pulses which make up a superframe. Note for superperiod mode these limits should be set to off and some care should be taken when setting these values for superframe mode. See notes later on.

Apart from the TRS parameters we also will make some comments about some of the TOF parameters which may be useful when constructing TRS experiments.

There are in fact only two subroutines which are called to deal with the TRS parameters, these are RUNTRS and OFFTRS. The first transfers the values to the relevant registers in the DAE to control the TRS hardware and the second clears all of those registers and sets the TRS hardware to "off". These two routines in turn call two other subroutines, PUTREG and GETREG, which are routines which given a register address

and a value, literally write the value to the DAE. The listings for these subroutines are given in appendix B. They are called from the subroutines SETMON and SET in the PRISMA operating program code. The SETMON subroutine is the one that deals with beginning and ending runs, pausing them once a set number of frames has been passed and then resuming when the relevant spectrometer movement etc. has been carried out. The SET subroutine is the one that "sets" values for parameters in the PRISMA program. Normally if a value is set it is not used until a run begins or a movement takes place, i.e. setting a parameter does not cause something to happen. However in the case of the TRS if the TRS system is switched off (see next section) these instructions are sent to the DAE straight away via the SET command.

5.2 The EON Parameter

A point to note which applies to all of the following modes set by the EON parameter is the following. When PRISMA/ISIS are not "running", i.e. if ISIS goes off, if the counting is paused or during the time between runs, the software has been set up to send a field-off (or low) signal out from the TRS to the external field. This is done for safety considerations. NOTE: A user should not rely on this, and should take whatever precautions are necessary to ensure that any external field etc. is safe before they seek to interact with the field equipment. Having made the point that it is the users responsibility to ensure safe operation of the equipment, not the computer programmes responsibility, we note that it is possible using manual switches in the HVS system to leave the external field turned on if so desired. The EON parameter can take 5 values which have the following effects.

- **EON = 0** : This is the normal operation mode of the PRISMA spectrometer. The TRS hardware is switched off.
- **EON = 1** : This is the superframe mode of operation.
- **EON = 2** : This is the superperiod mode of operation.
- **EON = -1** : This is a diagnostic mode of operation. The circuitry within the TRS to generate superframes, delays etc. will run but the output signal to the external field will be permanently low (i.e. off).
- **EON = -2** : Although in principle a diagnostic mode of operation, this mode can be useful for experimental work. The output signal to the external field is held high (i.e. on) at all times during the run. Although the superframe circuitry will run, it's effect on the sample is nil since the field is permanently on. Note the above caution, if paused, or if ISIS goes off then the field will go off, even in this EON = -2 mode.

5.3 The DELAY Parameter

As noted earlier DELAY takes the value of the delay time in microseconds. Note this must be in quanta of $10\mu s$ units, i.e. delay times of 0, 10, 20, $10020\mu s$ are allowed but not 3, 9 , $10021\mu s$. The name of the DELAY parameter can be abbreviated to DEL if so desired.

When calculating the value of the delay time from equation 4 it is possible to end up with a negative value, if the real time δ exceeds the time at which the neutrons were at the sample T_S which is given through the Bragg scattering condition. In other words effectively the field needs to be turned on *before* the neutrons leave the target/moderator. This is not an impossible thing to do, add 20ms to the delay time calculated from equation 4 which, since the latter is negative means the new delay time you calculate will be less than 20ms. In other words you're using the previous neutron pulse to trigger the external field. This will work fine if your superframe is two or bigger because the window limits described below will ensure that all the ISIS pulses stay in register/synchronisation with each other. You just have to think carefully about what real time each frame within the superframe corresponds to, effectively the first frame turns out to be the longest in real time now and the others all need to have 20ms subtracted off. If this is done with a superframe length of one then it is more dodgy because the window limits will not ensure the frames remain in synchronisation.

5.4 The DURAT Parameter

As noted earlier DURAT specifies how long the external field is turned on for. As with DELAY the value for DURAT is given in microseconds but must be in quanta of 10μs units.

5.5 The SFRAM Parameter

This parameter specifies how many ISIS 20ms frames should make up the superframe. It can take any value from 1 up to 65535, it should not be set to zero under any circumstances. There are a number of cases to be considered.

- Firstly if the TRS system is not being used at all, i.e. EON=0, then SFRAM should be set to 1.
- Secondly if the TRS system is being used but the timescales are all within 20ms it is quite possible to work with SFRAM=1, i.e. a superframe length of only 1 ISIS frame. This should "look" the same as any other superframe to the user with the exception that the window limits (see subsection(5.6)) should be switched off. In the software code and the TRS hardware a superframe of 1 does have to be treated differently to superframes of 2,3,..., etc. but to the user it should look the same.
- In superframe mode EON=1, SFRAM can take any value from 1 up to 22, the latter being the largest superframe the DAE can handle.
- In superperiod mode EON=2 the SFRAM value should be equal to the product of the number of periods (N_{sp}) in the superperiod times the number of frames in a period array element (F2P). It should be noted that this is the superframe length corresponding to the superperiod. The superframe length, i.e. SFRAM, being the cycle time/length in units of ISIS frames for the external field.

5.6 LWIN and UWIN - The Window Limit Parameters

When a superframe is created a series of ISIS frames are daisy-chained together. An ISIS frame starts when the accelerator extracts protons from the synchrotron and fires them at the target. The time between pulses is a frame. It should be noted that this time between pulses is not precisely 20ms (we've found that statistically it is more like $19999.80 \pm 0.02\mu s$ and it can fluctuate if the accelerator misfires or such like. Under normal operation EON=0 this variation of the frame length doesn't actually matter. If a frame is slightly shorter than 20ms the DAE electronics will be reset by the next pulse from ISIS and if it is slightly longer than 20ms the DAE will just ignore the extra data beyond 20ms and just wait for the next reset.

In a superframe however such a discrepancy in the frame length would be a serious problem since it would lead to a "blurring" of the real time scale. In order to eliminate this effect in superframe mode a "limit window" is used. When the superframe is started the TRS hardware uses its own clock to check that the ISIS frames which make up the superframe are all started at the correct time within a tolerance given by +UWIN and -LWIN in μs. If the ISIS pulse (start of the ISIS frame within the superframe) falls outside this time window the superframe is vetoed. This check is of course not applied to the first frame in the superframe, since this the pulse that creates this frame is the starting gun for the superframe (i.e. it is the pulse that starts the clock in the TRS). Note if the superframe is vetoed due to the ISIS pulses wandering the TRS system will require ISIS to successfully complete two whole superframes before it will allow the DAE to record data again. This is to ensure that ISIS is stable again before trying to collect superframe data.

The upper (UWIN) and lower (LWIN) time limits are set separately and we have found that it is better to bias to a larger LWIN rather than UWIN (frames are more often a tiny bit shorter than they are a tiny bit longer). It should be noted that LWIN and UWIN can be set in 0.2 μs steps but that there is the restriction that LWIN + UWIN $\leq 25.6\mu s$.

In superperiod mode these limit windows should be set to off, i.e. no checking is done. This is achieved by setting LWIN = 0 and UWIN = 0. Since in superperiod mode the real time scale has been "blurred" by at least 20ms by grouping the frames into periods anyway the μs blurring due to frame length variation is irrelevant. It is also the case that for the much longer real times used in superperiod mode rather than superframe mode the synchronisation of the ISIS pulses would nearly always exceed the 25.6 μs upper limit of LWIN + UWIN and one wouldn't collect any data with the windows active.

5.7 The HARDPERIODS.DAT file

While the superframe parameters can be set within the PRISMA program the parameters for a superperiod measurement must be provided by a file known as the HARDPERIODS.DAT file. This file should be placed in INST_TABLES where the ICP program can find it when a superperiod measurement is started. A program exists HWRIT to create this file. Although the structure of the file is simple, repetitively typing in numbers can be tedious and can cause errors, hence HWRIT does this for the user. The values in HARDPERIODS.DAT are simply a column of numbers. The first value is the number of periods (memory locations) in a superperiod and the second is the number of frames in a period array element (F2P). This is followed by 256 element array of values indicating in

which period each block of F2P frames is to be stored. Note this map of 256 values must be cyclic and commensurate with the value of 256. An example of a set of values for a HARDPERIODS.DAT file might be;

5 4 1 2 3 3 4 4 5 5 1 2 3 3 4 4 5 5 1 2 3 3 4 4 5 5 ....

(The numbers in the file should be in a column not a row.) The first value, 5, indicates that 5 periods (locations in memory) are to be used. The counting unit in frames is 4 (the second number). The remaining numbers are the mapping of blocks of 4 frames to periods, which is cyclic with a repeat of 8. If we think about what happens as frames of data come into the DAE then the above pattern becomes clearer. The first 4 frames that come in are all stored in period 1 which then contains an average over the first 80ms. The next 4 frames that come in are stored in period 2 which hence contains an average over the time from 80ms to 160ms. The next 4 frames that come in are stored in period 3, but then so are the next 4 frames after that as well. Thus period 3 contains an average over times from 160ms to 320ms. Similarly period 4 covers 320 to 480ms and period 5 covers 480 to 640ms. After the second 5 in the list we have completed our 8 array elements and we have used up a total of 32 (i.e. 8×4) ISIS frames. Thus the superframe length is 32 and the SFRAM parameter should have been set to 32 in the PRISMA program. At this point the superperiod (and superframe) are complete. The TRS hardware will reset the external field and the whole procedure starts again, i.e. the 8 values are repeated in the list. When all 256 values are completed the list just starts again at the beginning. This is why the cycle of period locations must be periodic in 256, i.e. you can only choose the length of the cycle to be 1, 2, 4, 8, 16, 32, 64, 128 or 256. There are obviously many ways of configuring such a set-up in order to try and optimise the resolution of the real time information vis-a-vis other constraints. A serious constraint which has not been mentioned is the amount of DAE memory that will be used, remember for every period a set of spectra (detectors and monitors times the number of time channel boundaries) must be stored. Note the double mapping, e.g. 3 3 4 4 5 5, used in the example above along with the the use of ranges of time channels (see subsection(5.8)) can be used to minimise the amount of memory required. In practice the authors have so far only used a "simple" superperiod structure, one detector and a 1 to 1 mapping of cycle elements to periods, e.g.

128 1 1 2 3 4 5..... 127 128 1 2..... 128
64 4 1 2 3 4..... 64 1 2..... 64 1 2..... 64 1 2..... 64

The HWRIT program will write the HARDPERIODS.DAT file. When run it prompts the user with the following questions

Enter the nos of periods: **5**
Enter the nos of frames per array element : **4**
Enter the nos of array elements (2,4,8...) : **8**
Enter the period for each array element
Element 1 : **1**
Element 2 : **2**
Element 3 : **3**
Element 4 : **3**
Element 5 : **4**
Element 6 : **4**
Element 7 : **5**
Element 8 : **5**

Note the bold numbers do not appear of course, they are the answers that would have been given to create the HARDPERIODS.DAT file used in the first example. After the last (8th in the example) value has been typed in HWRIT creates the HARDPERIODS.DAT file with the correct number of repetitions of the 8 elements. It also prints out the superframe number to be used for SFRAM in the PRISMA program.

5.8 The ToF parameters in the PRISMA program

Although no new time of flight parameters are introduced for TRS experiments some comments on how these paramters are set for real time experiments is perhaps appropriate. The TOF family of parameters are

- **MNT** — The type of monitor count.
- **MNS** — The size of the monitor count.
- **BIN** — The selection of the counting time ranges.
- **START, STOP, STEP** — The definition of the times at which the counting starts, stops and the size of the counting channels.
- **STOP2, STEP2** — Definitons of the stop times and size of the counting channels for subsequent time ranges.

The MNT parameter is usually set to either 0 (count forever, i.e. until the run is ENDed) or 1 count for a fixed number (MNS) of frames. The MNS parameter is the number of ISIS frames or superframes for which the count should be performed. If EON=0 (i.e. normal operation) or EON=2 (i.e. superperiod mode) the value of MNS will be the number of ISIS 20ms frames for which the count should be performed. Note in these two modes the frames displayed and the ISIS current on the "dashboard" should be the operating value for the accelerator (e.g. 50Hz and 200 μA). If however EON=1 (i.e. superframe mode) then MNS will be the number of superframes for which the count should be performed. On the dashboard the frequency of ISIS, the nos of frames and the ISIS current will be scaled down by a factor of n where n is the nos of ISIS 20ms frames in a superframe.

The BIN parameter sets the number of "ranges" over which the time of flight channels are constructed. It is on most occassions set to BIN=1. If BIN=0 is set then the time of flight channels used are those set using the CHANGE command via the ICP. If BIN=1

then three parameters are used to define the time channel boundaries, START — the time in μs when counting should start, STOP — the time in μs when it should stop and STEP — the size of the time channels between START and STOP in μs. Under normal operating conditions START and STOP are between 5 and 20000 μs and STEP can be in 1 μs units or higher multiples. Similarly in superperiod mode one is effectively working within 20ms ISIS frames and the same criteria apply. In superframe mode STOP might be any allowed value up to 440000 μs. The quantum unit, i.e. smallest allowed value, for STEP depends on the size of the superframe. A quantum unit of 1 μs can be used for superframe lengths up to 32ms, 2 μs for superframes up to 64ms, 3 μs for superframes up to 96ms and so on up to 14 μs for superframes up to 440ms. If the value of BIN is greater than 1 then extra STOP and STEP values must be defined. If for example BIN=2 then the values START, STOP, STEP, STOP2, STEP2 must be defined. the time channels are then constructed from START to STOP in channels of size STEP and from STOP to STOP2 in channels of size STEP2. Values of BIN can be used up to a maximum of 9 if so desired and the corresponding STOP and STEP values up to STOP9 and STEP9 must be defined.

5.9 Data Analysis GENIE Macros

There are 3 GENIE macros (.com files) which are useful when analysing data taken in TRS mode. The first is TDD4 which allows spectra within a raw file taken in superframe or superperiod mode to be displayed. It is very similar in function to the DD (DD4) macro in the normal set of PRISMA data analysis programs [4]. Also there are ASF4 and ASP4 which allow spectra taken in superframe and superperiod in different runs to be integrated over a limited range (e.g. a Bragg peak) and stored in a file as a function of delay time, frame number or period number ready for plotting or further analysis. Each of these three macros will be described in turn.

5.9.1 TDD4:==@PRISMA_KNH_COM:TSPACE4.COM

This GENIE macro can be used to display the diffraction spectrum from a particular frame or period in either (1) wavelength, (2) incident energy, (3) d-spacing, (4) time of flight, (5) wavevector transfer. Note the 4 at the end of the TDD4 indicates that this routine is written specifically for the PRISMA-4 diffraction detector. In other words one must enter the specific detector tube used and the macro will then use the correct sample to detector distance. TDD4 is very similar to the DD4 macro which is just the PRISMA-4 version of the DD macro described in the PRISMA GENIE Data Analysis Manual [4]. The difference is that TDD4 includes extra code to select out the particular frame or period within a superframe or superperiod.

When TDD4 is run it first prompts for the run number to analyse. The next two prompts are for the total number of detectors *being counted* and the actual detector for which you wish to carry out the analysis. The answer to the first question is the number of detectors in which you actually collected spectra (often this might just be 1) and not the total number of detectors in PRISMA-4. The answer to the second question is literally the tube/detector number, so that the correct final flight path distance is used.

The next prompt is for the type of analysis to be carried out, do you want to display the spectrum in (1) λ, (2) E_i, (3) d, (4) ToF, (5) Q. If you select (3) or (5) you will

then also be prompted for the absolute value of the scattering angle for the particular detector. The next two prompts are the minimum (lower) and maximum (upper) limits over which the spectrum will be displayed. The following prompt is the bin size to be use when rebinning the raw data between the minimum and maximum limits. Note these three values should be in the relevant units (1) Å, (2) meV, (3) Å, (4) μs, (5) Å^{-1}.

The next prompts are for the superframe number, the spectrum number corresponding to the detector used and the point number in a step scan. If the scan was taken in superframe mode and was just a single setting enter 1 for the point number. If this was a superperiod run then enter 1 for the superframe number and enter the number of the period you wish to display for the point number. Note in superperiod mode you cannot perform a step scan. After this the spectrum will be displayed on the graphics device between the minimum and maximum limits specified. After returning from the graphics plot the integral of the spectrum between the minimum and maximum limits will be given on the alpha screen. Note the integral and spectrum plotted have been normalised so that the integral of the monitor 1 spectrum between 1000 and 12000 μs is equal to 100000.

At this point a menu of options is presented, (1) EXIT, (2) DIFF DET/POINT/SFRAME, (3) DIFFERENT RUN, (4) K/H LAST PLOT, (5) PLASER7 LAST K/H OR PRESS RETURN FOR NEXT POINT, all of which are fairly self explanatory.

5.9.2 ASF4:==@PRISMA_KNH_COM:ANATIM.COM

This GENIE macro can be used to integrate spectra from within a superframe run in either (1) wavelength, (2) incident energy, (3) d-spacing, (4) time of flight, (5) wavevector transfer and produce a formatted output data file of the results. An auxillary file DELS.DAT can be provided for the analysis which is simply a column of numbers listing the delay times or real times for each of the relevant final results. Note these values are only used in the final output file (as the x-values).

The prompts for ASF4 are very similar to those for TDD4 with the same meaning. Just the differences will be described. Initially when the ASF4 macro is run it prompts for the first and last run numbers to process (TDD4 of course only prompted for one run number). All the run numbers between the first and last entered will be processed. The following prompts are the same as for TDD4 until the prompt for the number of superframes (in TDD4 this was a prompt for the superframe number). The answer to this prompt is the total number of ISIS frames within the superframe. The next promts are for the detector spectrum number and point number as for TDD4.

After these values are entered the macro then carries out the analysis of each of the runs. Note as for TDD4 the data is normalised to a monitor 100000 between 12000 μs. The integration of the detector spectra is carried out between the minimum and maximum limits entered. The results are stored in an intermediate file called TRSTOR.DAT. Note results are appended to this file and the file is not deleted when the macro is completed. Thus if further runs are to be analysed and merged with earlier ones they can be done so by just running the macro again. If a new analysis is to be carried out then this file should be deleted or renamed. The storage of the results is carried out by a FORTRAN program called STOFIL running within GENIE. An example of the contents of a TRSTOR.DAT file is given below, the columns are run number, frame number, counts and error in counts.

```
16232    1    93.91    2.52
16232    2    97.49    2.56
```

16232	3	104.27	2.65
16232	4	100.74	2.61
16232	5	94.46	2.52
16233	1	96.12	2.54
16233	2	95.28	2.53
16233	3	100.20	2.59
16233	4	94.25	2.51
16233	5	96.03	2.54
16234	1	93.23	2.51
16234	2	96.37	2.55
16234	3	98.58	2.58
16234	4	97.21	2.56
16234	5	95.39	2.53
16235	1	94.41	2.52
16235	2	91.31	2.48
16235	3	100.71	2.61
16235	4	99.07	2.59
16235	5	96.42	2.55

Once all of the runs have been processed, another FORTRAN program TRSORT is run by the macro within GENIE to combine together different runs and average the results and errors to produce a final output file in the format given below

RUN	DELAY	I1	E1	I2	E2	I3	E3	I4	E4	I5	E5
16332	-0.050	233.8	4.0	237.4	4.0	271.3	4.3	268.4	4.3	228.6	3.9
16333	-0.040	232.1	3.9	238.3	4.0	271.8	4.3	272.9	4.3	227.4	3.9
16334	-0.030	235.1	4.0	229.4	3.9	273.8	4.3	266.2	4.2	227.6	3.9
16335	-0.020	232.8	3.9	229.5	3.9	276.8	4.3	258.8	4.1	232.0	3.9
16336	-0.010	230.5	3.9	231.3	3.9	271.7	4.2	249.1	4.1	229.4	3.9
16337	0.000	228.5	3.9	227.5	3.9	271.7	4.2	252.0	4.1	229.2	3.9
16338	0.010	238.5	4.0	224.9	3.9	273.3	4.3	242.9	4.0	230.4	3.9
16339	0.020	229.9	3.9	235.9	4.0	272.2	4.3	224.6	3.9	228.8	3.9
16340	0.040	234.9	4.0	227.6	3.9	261.7	4.2	224.3	3.9	224.1	3.9
16341	0.060	226.6	3.9	233.8	4.0	258.8	4.2	227.4	3.9	232.0	3.9
16342	0.080	229.2	3.9	234.2	4.0	271.5	4.3	234.0	4.0	226.7	3.9
16343	0.100	231.1	3.9	229.7	3.9	267.9	4.2	239.2	4.0	232.2	4.0
16344	0.120	222.9	3.9	239.2	4.0	259.7	4.2	236.1	4.0	235.9	4.0
16345	0.140	227.8	3.9	237.0	4.0	267.0	4.2	233.5	4.0	230.3	3.9
16346	0.200	227.8	3.9	244.9	4.1	261.5	4.2	227.4	3.9	229.3	3.9
16347	0.300	224.6	3.9	264.2	4.2	263.0	4.2	221.1	3.8	226.2	3.9
16348	0.400	231.7	3.9	256.1	4.1	268.4	4.2	225.2	3.9	228.2	3.9
16349	0.500	229.9	3.9	261.2	4.2	257.5	4.1	224.0	3.9	223.9	3.9
16350	0.600	231.0	3.9	263.1	4.2	264.2	4.2	220.2	3.8	223.9	3.9
16351	0.800	233.4	4.0	255.8	4.1	267.5	4.2	226.1	3.9	231.1	3.9
16352	1.000	224.9	3.9	270.7	4.2	264.3	4.2	224.1	3.9	227.4	3.9
16353	1.500	228.8	3.9	259.2	4.2	265.5	4.2	230.7	3.9	224.9	3.9
16354	3.000	229.8	3.9	264.4	4.2	261.4	4.2	229.3	3.9	226.4	3.9
16355	3.500	232.5	3.9	255.1	4.1	271.6	4.3	223.8	3.9	226.6	3.9

Note in this example the delay times are given in milliseconds. This file can be plotted using input option 4 in the SPLOTG program or any other plotting program which can take the input format.

5.9.3 ASP4:==@PRISMA_KNH_COM:ANAPER.COM

The ASP4 macro is very similar to the ASF4 macro but ASP4 deals with superperiod data. In fact the input prompts are identical to those of ASF4 with the exception that instead of prompting for the number of frames in a superframe the ASP4 macro prompts for the number of periods. This is the number of separate storage locations in memory, i.e. the first number in the HARDPERIODS.DAT file. If we were analysing the data taken using the first example in subsection(5.7) then the answer would be 5 (not 8). As each run is processed the data is stored by the FORTRAN program STOFIL. Once all of the runs have been processed the FORTRAN program TRAVER produces the final output file, an example of which is given below, the three columns are period number, counts and error

```
 Output from superperiod runs
64
     1    138.14      1.63
     2    135.97      1.51
     3    144.30      1.55
     4    151.47      1.60
     5    151.51      1.59
     6    149.04      1.60
     7    149.39      1.60
     8    150.20      1.61
     9    153.24      1.61
    10    152.04      1.63
    11    152.42      1.63
    12    146.11      1.60
    13    144.95      1.59
    14    143.02      1.59
    15    141.06      1.59
    16    141.72      1.59
    17    141.49      1.58
    18    139.75      1.59
    19    141.75      1.59
    20    141.69      1.61
    21    138.12      1.58
    22    139.82      1.61
    23    138.89      1.60
    24    138.57      1.60
    25    137.42      1.58
    26    139.04      1.62
    27    138.92      1.61
    28    139.74      1.63
    29    139.74      1.62
```

30	139.19	1.63
31	137.64	1.63
32	138.83	1.64
33	136.40	1.61
34	139.10	1.64
35	138.88	1.64
36	137.79	1.64
37	137.28	1.64
38	141.01	1.67
39	139.77	1.67
40	137.58	1.66
41	138.77	1.66
42	135.52	1.66
43	136.13	1.66
44	136.77	1.67
45	140.47	1.68
46	137.97	1.68
47	138.24	1.68
48	137.32	1.69
49	136.08	1.67
50	137.44	1.70
51	140.82	1.71
52	136.33	1.70
53	135.32	1.68
54	137.80	1.72
55	134.81	1.69
56	136.97	1.72
57	139.28	1.72
58	135.15	1.72
59	139.42	1.74
60	136.80	1.74
61	140.08	1.75
62	135.51	1.74
63	137.06	1.74
64	136.84	1.75

5.10 The Diagnostic Programmes REGRED and REGSET

These two programmes were written for diagnostic purposes during the development of the TRS system. One of them REGRED, reads and outputs the value of a register in the DAE and the other REGSET writes a value to a register in the DAE (it also re-reads the value to check it has been set). Listings for these two programmes and also the link command (REGLINK.COM) for them are given in appendix B. The prompts and output for the two programmes are self sxplanantory when they are run and consist of the register address and value.

A Circuit Diagrams

This appendix presents the 8 Xilinx circuit schematics which together make up the TRS system. Each schematic is described in a separate section which explains how that part of the TRS system works and how it interacts with the other subsystems. Components in these schematics which are referred in the text are given labels which identify the component by the grid square in which the component is located plus the component type and the subsystem to which the component belongs. For example in the section describing the comparator subsystem the component labeled in the text as 4OR.B5 is an OR gate and the location of the component is grid square B5 of that schematic. Likewise the component 5FF.D5 referred to in the superframe register section is a flip-flop located in grid square B5 of the superframe register schematic. In each schematic the grid squares range from A1 which is the bottom right hand square to D8 which is the top left hand square. The first number in each label is the ID code number of the particular subsystem to which the component belongs. The subsystem ID codes and the sections which describe each subsystem are as follows

- Top schematic - section A.1
- Register control and clock distribution - section A.2, ID code 1
- System control - section A.3 , ID code 2
- Limit generator system - section A.4, ID code 3
- The comparator system - section A.5, ID code 4
- The superframe register - section A.6, ID code 5
- The external field control system - section A.7, ID code 6
- The watchdog system - section A.8, ID code 7

Note that in the description of the TRS system given in chapter 4 the first two systems in the list (after the top schematic) were described as a single system that being system and register control. However the amount of circuitry that makes up this one system requires the use of two schematic diagrams to lay the components out and so system and register control as been appropriately split into two schematics and hence two sections.

A.1 The Xilinx Schematics

The top schematic of the TRS system is shown in figure 16. The input and output signals shown in the figure are organised as follows. On the left of the TRS block is the main 16 bit data bus DATA_TR. Located above this data bus are all the read and write signals which fed from the address decoder boards in the DAE. Below the data bus are the main three inputs to the TRS system. These carry the 50Hz ISIS pulses from the proton pulse sensor, the DAE_RUN signal from the DAE which tells the TRS system when PRISMA has started a run, and the 10MHz master timing signal M_CLK.

On the lower right hand side of the TRS block are the four main outputs of the TRS system. These are the DAE output line which sends the superframe or 20ms ISIS pulses

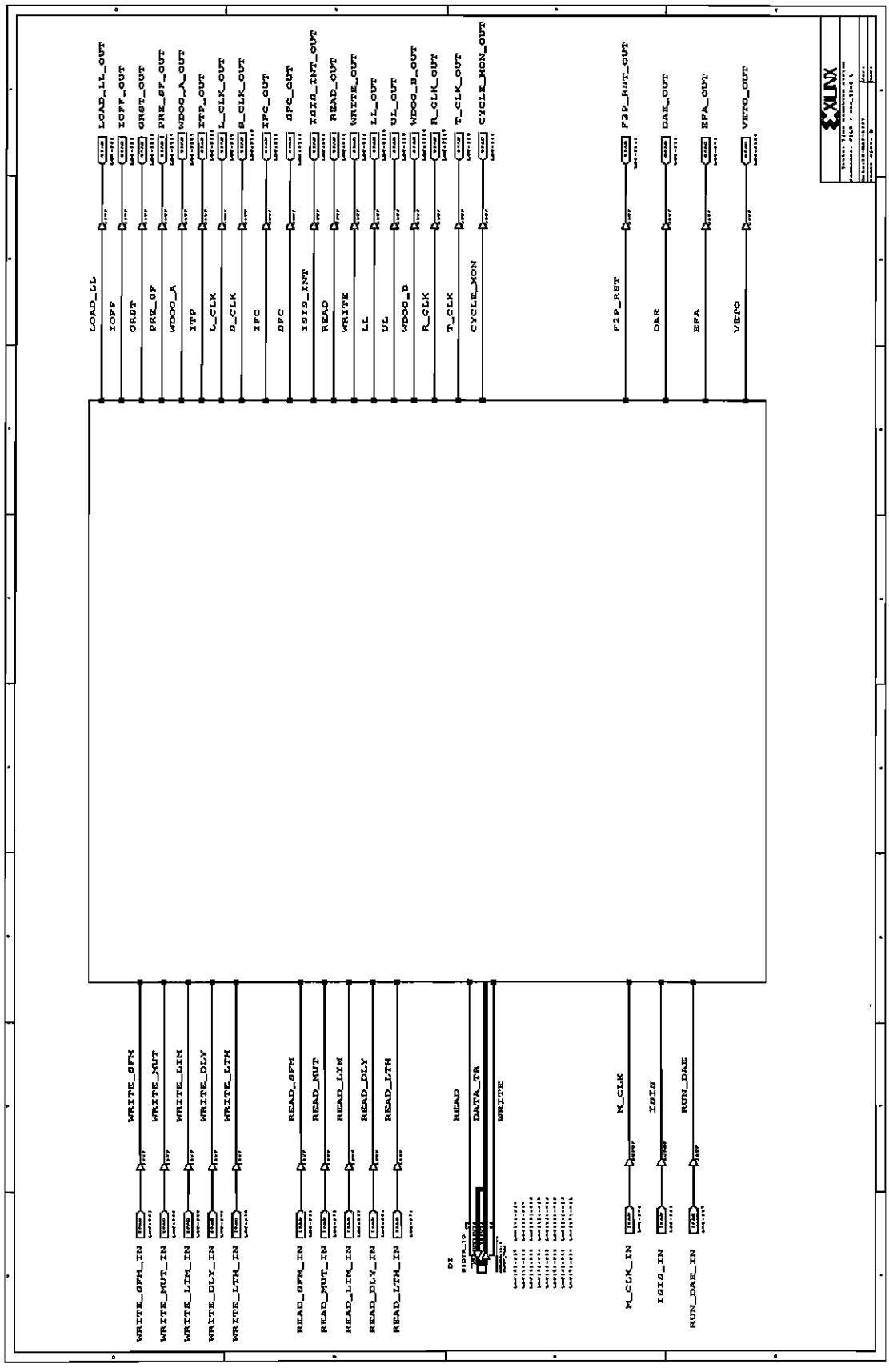

Figure 16: Top level Xilinx schematic for the TRS system

to the DAE depending on which mode (superframe or superperiod) the TRS system is operating in. There is the EFA line which is used to send the EFA trigger pulse to an separate external field system which is used to apply an external field to a sample. There is the VETO line which goes to the DAE and which causes the DAE to reject data stored in its temporary memory in the event of a synchrotron failure. Finally there is the F2P_RST line which is used in the superperiod mode to reset the 8-bit period counter in the DAE if a fault occurs with the synchrotron. The remaining outputs are all monitoring points used for test and diagnostic purposes.

A.2 Register Control and Clock Distribution

The register control and clock distribution circuit (figure 17) carries out two main functions. The first function it performs is to divide up the 10MHz clock signal, which is fed to the TRS system from an external oscillator, into 3 further clock signals, a 5MHz, a 1MHz and a 10KHz clock signal. All four clock signals are then fed out to the rest of the TRS system where they are used for a variety of different functions. These functions are fully described discussed at the relevant point in this appendix. The second function of this circuit is to control the read and write signals for the five data registers that exist within the TRS system. These data registers are used for example to set the length of superframe and the delay time and length of the external field pulse. The data for these registers are sent from the instrument control computer to the TRS system via a data bus in the instruments DAE. This data bus feeds the main 16 bit data bus within the TRS system which itself is connected to the D_IN input of each of the 5 data registers. The task of the register control and clock distribution circuit is to load the correct register with the correct data when that data is sent from the instrument computer.

A.2.1 Clock Distribution

The TRS system is supplied with a highly accurate (to 1 part in 10^8) and stable 10MHz clock signal from a crystal oscillator which is mounted next to the Xilinx chip as shown in figure 5 and described in section 3.1. This 10MHz signal (labeled M_CLK) is subdivided into 3 further frequencies by three clock dividers. One clock divider, 1CD.B7, produces the 1MHz signal, T_CLK, which is used to generate a number of signals like the LL, UL pulses from the limit generator circuit. A second clock divider, 1CD.A6, uses the T_CLK clock signal to produce the 10KHz R_CLK signal which is used in the part of system control (section A.3) that is responsible for monitoring the ISIS pulses from the proton pulse generator. Finally a 5MHz clock signal S_CLK is produced by clock divider, 1CD.A7, which is used to drive the limit generator circuit (section A.4.1, figure 19) and the electric field control system (section A.7, figure 22).

A.2.2 Data Load/Read

The five data registers used in the TRS system can be found in the following subsystems. Data register 3RG.B7 (address 2166) is located in the limit generator system (section A.4). Data Register 6RG.D4 (address 2168) and 6RG.B4 (address 2170) are to be found in the electric field system (section A.7), and data register 5RG.B7 (address 2172) is located in the superframe register (section A.6). The last data register 1RG.C3 (address 2164) is part of this system i.e. the register control and clock distribution network.

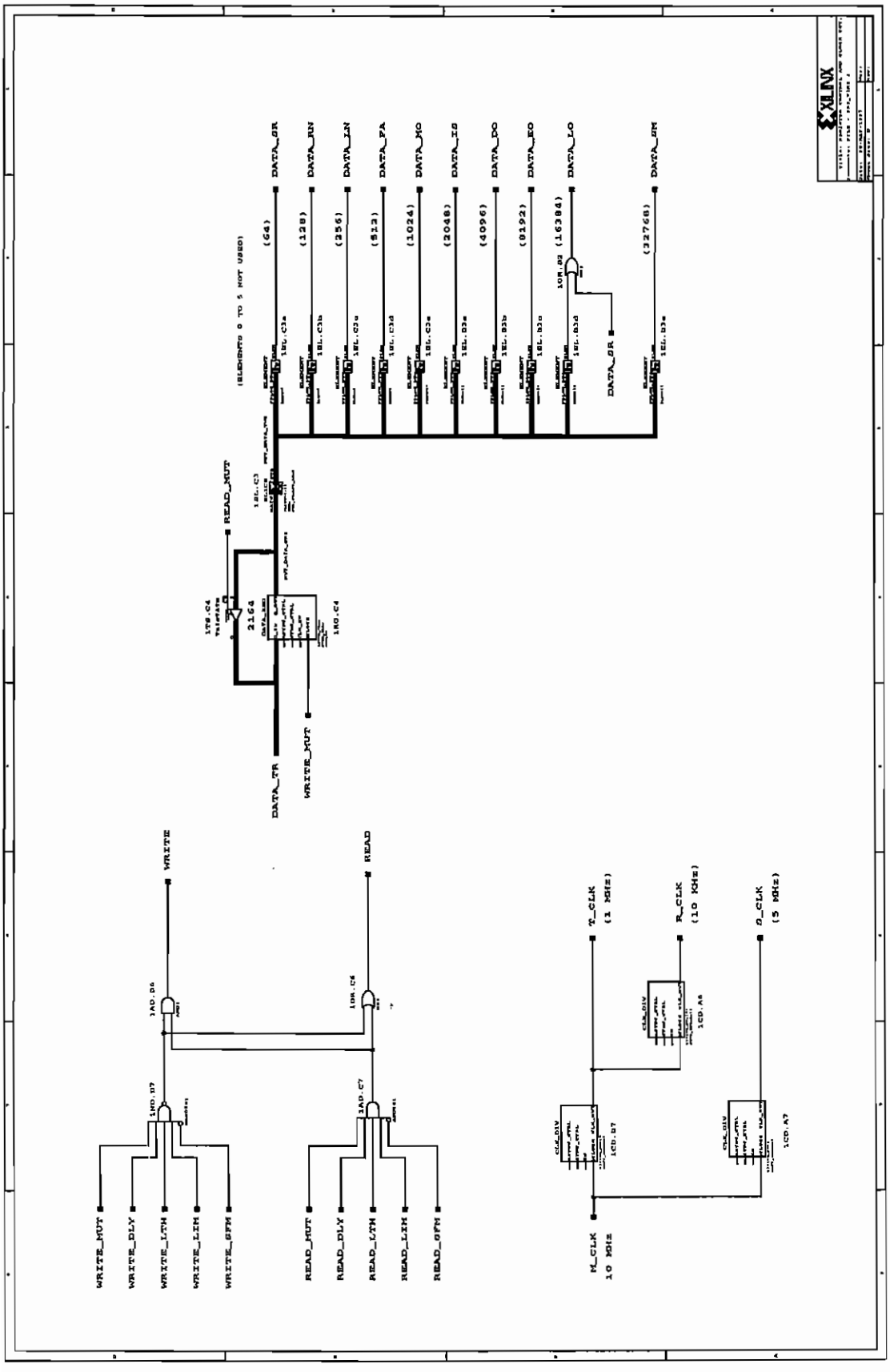

Figure 17: Xilinx schematic 2 - register control and clock distribution

All five data registers are loaded by the action of the WRITE_* signals (* = MUT, DLY, LTH, LIM or SFM) which are used to drive the clock inputs of the data registers (see for example data register 2164). These signals, and the relevant data registers, are listed below

- WRITE_MUT (and READ_MUT) = Register 2164
- WRITE_DLY (and READ_DLY) = Register 2168
- WRITE_LTH (and READ_LTH) = Register 2170
- WRITE_LIM (and READ_LIM) = Register 2166
- WRITE_SFM (and READ_SFM) = Register 2174

These WRITE_* signals also make up the 5 inputs to gate 1ND.D7 in figure 17. The signals are normally held in a high state, going (active) low for ~400ns when the address decoder circuits within the instruments DAE are activated. The Xilinx FPGA is mounted on the circuit board in the DAE that holds the address decoder logic for the DAE's own registers. This circuit board offered 10 spare address lines (5 read and 5 write) which are now used by the TRS system.

To illustrate how a register is loaded and read consider data register 2164 (location 1RG.C4) which is clocked by the WRITE_MUT signal. When the WRITE_MUT signal, from the DAE'S address decoder circuit board, goes low, the output of 1ND.D7 rises to a logic 1 enabling AND gate, 1AD.D6. The other input to 1AD.D6 is from the output of gate 1AD.C7 which is high since all the READ lines are held at a logic 1 level in the absence of a read command. Actually READ_SFM and WRITE_SFM have the reverse logic of the other read and write signals. To correct this difference there are inverters on the relevant inputs of gates 1ND.D7 and 1AD.C7. The WRITE signal enables the input buffer on the bi-directional gate D1 (see top figure 16) allowing data to be gated onto the main data bus in the TRS system (DATA_TR) from the DAE data bus (not shown). The data on DATA_TR will be present at the D_IN inputs of all 5 data registers, however only the WRITE_MUT signal is active (only address 2164 has been selected) in this example. When, after 400ns, the WRITE_MUT signal returns to a logic 1 level the positive going edge will trigger the data register 2164 thereby clocking the data from bus DATA_TR into the register 2164. This data will then appear at the output of data register 2164 on the bus MUT_DATA_ONE. To read back the data the relevant READ_* line (READ_MUT in this example) will go low for 400ns placing a low on the READ line and an inhibit on gate 1AD.D6. This low enables the output buffer of the bi-directional gate D1 in figure 16, and also enables one of 5 tri-state components (one for each data register) which, in this example, is 1TS.C4. The tri-state device gates the contents of the data register output back onto the bus DATA_TR and hence out of the Xilinx chip via the enabled Bi-Directional gate an onto the DAE data bus which can then be read by the instrument computer. All 5 data registers work in this manner.

A.2.3 Data Register '2164'

This is a multi-task Data Register that controls all the functions of the TRS system. The 16 bit output of the register is split into 10 single data lines, which are lines 6 to 15 (lines

0 to 5 are not used), by the element components 1EL.B3a to 1EL.C3e. The functions of these lines when active high are listed below.

DATA_SR Element 1EL.C3a. The DATA_SR signal is used in the superframe register (section A.6) to place the TRS system into the superperiod mode. The superperiod mode is selected by adding decimal 64 to the contents of data register 2164.

DATA_RN Element 1EL.C3b. The EFA signal from the electric field control system (section A.7) can normally only be produced if (a) the instrument is in its run mode and (b) the ISIS neutron source is running normally. The DATA_RN line is fed to the electric field control system where it allows a permanent (not pulsed) EFA signal to be produced even when the instrument is in its standby mode or ISIS has failed. This option is selected by adding decimal 128 to data register 2164.

DATA_LN Element 1EL.C3c. The frequency of the UL and LL pulses from the limit generator (see section A.4.3) is not exactly 50Hz, but rather it is tuned to the frequency of the ISIS pulses. Selecting this option runs the limit generator independently from the rest of the TRS system so that adjustments to the limit generator frequency can be made before the rest of the TRS system is activated. The details of this procedure are contained in the limit generator section (sectionA.4.2). This option is selected by adding decimal 256 to data register 2164.

DATA_FA Element 1EL.C3d. If a permanent electric field is required rather that a pulsed field then this can be achieved by setting this line high (section A.7). This is not the same as DATA_RN since here the permanent EFA signal produced by this option is lost in the event of an ISIS failure or if the instrument is put into its standby mode. This option is selected by adding decimal 512 to data register 2164.

DATA_MO Element 1EL.C3e. This is the master override signal that, when low, overrides all functions of the TRS system and allows the ISIS pulses to pass through unimpeded (sections A.3 and A.6). When the TRS system is not being used the contents of data register 2164 would normally be set to zero thereby overriding the TRS system. To operate the TRS system either in the superframe or superperiod mode data register 2164 must at least hold the value decimal 1024.

DATA_IS Element 1EL.B3a. This is a test/diagnostic line which when set is used to simulate a synchrotron failure (section A.3) by preventing any ISIS pulses from entering the TRS system and hence preventing any of the ISIS pulses reaching the DAE. This option was used to check the reset circuits in the DAE and the TRS system and can be selected by adding decimal 2048 to data register 2164.

DATA_DO Element 1EL.B3b. The minimum programmable delay between the ISIS pulse and the appearance of the EFA trigger pulse for the external field is 20μs. This data line, when high, allows for a zero delay between the ISIS pulse and the EFA signal (see section A.7). This option is selected by adding decimal 4096 to data register 2164.

DATA_EO Element 1EL.B3c. This data line, when high, disables the electric field control trigger signal (EFA) while allowing the rest of the TRS system to function

normally (see section A.7). This option is selected by adding decimal 8192 to data register 2164.

DATA_LO Element 1EL.B3d. If the limit generator system is not required then setting this line high will disable the limit generator and the comparator systems (see section A.5). This option is selected by adding decimal 16384 to data register 2164. This option is also selected when the TRS system is running in the superperiod mode since the DATA_SR signal is gated through 1OR.B2 (output of 1EL.B3d) to produce the DATA_LO signal.

DATA_SM Element 1EL.B3e. The minimum programmable length of superframe is 2 ISIS pulses (i.e. 40ms). When high, the DATA_SM line sets the length of the superframe equal to one ISIS frame i.e. 20ms duration. This option is selected by adding decimal 32768 to data register 2164.

A.3 System Control

System control (figure 18) has three main functions. First it redistributes the ISIS pulses as 3 new signals. The first of these new signals is the ITP pulses which are sent to the comparator subsystem where their timing, and hence the performance of the synchrotron, is measured against the UL and LL pulses from the limit generator. The ISIS pulses are also redistributed as the ISIS_INT pulses which are used both in system control and the superframe register. finally the ISIS pulses are redistributed as the ISIS_ON pulses which are also used in system control and the superframe register and in addition they are sent to the watchdog circuit. Secondly system control is used to preload a counter in the limit generator with the data which governs the size and position of the limit window formed by the UL and LL pulses. To do this system control sends the LOAD_LL and L_CLK signals to the limit generator to load the counter with the data stored in register 2166 (see that section). This action of preloading the counter is performed at the start of each superframe. Lastly system control monitors the ISIS pulses looking for a synchrotron problem in the form of one or more missing ISIS pulses. If such a situation arises then it will issue the ISIS off signal (IOFF) which will reset the TRS system.

A.3.1 Operation

This description assumes that system control is reset at this time awaiting the arrival of the next ISIS pulse. When this occurs the ISIS pulses enter system control via the lower AND gate in grid B7. The other two inputs to this gate are the RUN_DAE and the DATA_IS signals. The DATA_IS signal is only used in certain test/diagnostic routines and is held low under normal operating conditions. The DAE_RUN line is active high only when PRISMA is running and therefore no ISIS pulses can enter the TRS system until a run has started. Assuming that a run has been started then the ISIS pulses are gated through the lower AND gate in grid square B7 to become the ISIS_ON pulses. These pulses are used both in system control and in the watchdog and superframe register subsystems. In the watchdog system they are used to drive an ISIS monitoring circuit and in the superframe register they become the 50Hz ISIS pulses to the DAE system when the superperiod approach is selected. See relevant sections for full details. In system control the ISIS_ON pulses are fed to one of the three inputs of the upper AND gate in grid

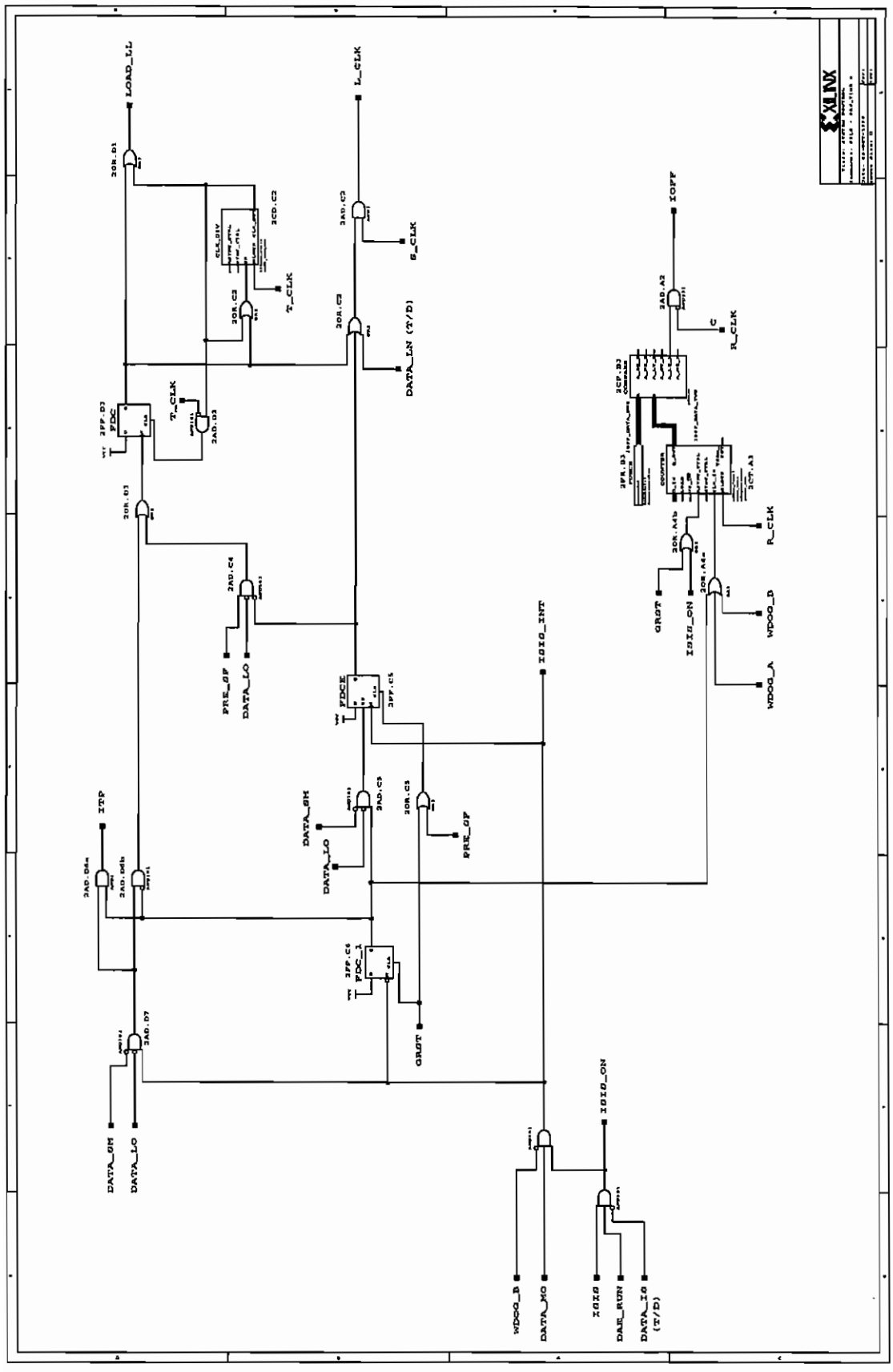

Figure 18: Xilinx schematic 3 - system control

square B7. The other two inputs to this gate are the WDOG_B signal and the DATA_MO signal. The DATA_MO (master override) signal is high when the TRS system is required and zero otherwise. The WDOG_B line will be set high if a synchrotron failure occurs which will then prevent the ISIS pulses from entering system control.

Assuming for now that the TRS system is required and the synchrotron is operating normally then the ISIS pulses will be gated through this AND gate to become the ISIS_INT pulses. These ISIS_INT pulses are used in two ways. First they are sent to the superframe register to be gated directly to the DAE system if the superperiod mode has been selected. Secondly they are used in system control to produce the ITP pulses for the comparator system as follows. When the first ISIS pulse is received by system control the subsequent ISIS_INT pulse will be routed to gate 2AD.D7 and flip-flops 2FF.C6 and 2FF.C5. The leading edge of the ISIS_INT pulse has no effect on the flip-flops because the CE (clock enable) input of 2FF.C5 is low at this time (because the Q output of 2FF.C6 is low) and 2FF.C6 is only set by a negative going edge. Therefore the only thing that happens at this time is that the ISIS_INT pulse is gated through 2AD.D7 since the other two inputs to this gate, DATA_SM and DATA_LO are both low. The DATA_SM line is only active when superframes equal in length to a single ISIS frame are required. It will be assumed for the moment that a superframe of 2 or more ISIS frames is required. The DATA_LO is active if the services of the limit generator and comparator subsystems are not required.

The first ISIS_INT pulse is gated through 2AD.D7 to the input of gates 2AD.D6a and 2AD.D6b. Gate 2AD.D6a is disabled because flip-flop 2FF.C6 is currently reset but the inverter at the input of gate 2AD.D6b means that the ISIS_INT pulse is gated through to clock flip-flop 2FF.D3. Setting this flip-flop produces the LOAD_LL signal via 2OR.D1 and enables gate 2AD.C2 allowing the 5MHz signal, S_CLK, to be gated to the limit generator as the L_CLK signal which together with the LOAD_LL signal will preload a counter in the limit generator (see section A.4).

At the end of the first ISIS_INT pulse the trailing edge of that pulse will set 2FF.C6 which will place an enable on gate 2AD.D6a (and disable gate 2AD.D6b) and an enable on flip-flop 2FF.C5. The next ISIS pulse into system control will be the first ISIS pulse of the superframe and as such must start the limit generator. It achieves this by setting the now enabled flip-flop 2FF.C5 which enables gate 2AD.C2 allowing S_CLK through to the limit generator as the L_CLK signal. This ISIS pulse must also switch on the comparator system by producing the first ITP pulse. This is now possible since gate 2AD.D6a is now enabled allowing the ISIS_INT pulse to be gated through as the ITP pulse.

For the duration of the superframe the ISIS pulses will be gated through system control to become the ITP pulses the timing of which is checked by the comparator to see if the synchrotron is functioning normally. If all is well then at the end of the superframe the superframe register will issue the PRE_SF signal which is used to switch off the production of the UL and LL pulses from th limit generator. The PRE_SF signal does this by resetting 2FF.C5 thereby removing the enable from gate 2AD.C2. The next ISIS pulse to enter system control will be the first of the next superframe and will enable this gate once more by setting 2FF.C5.

A.3.2 The IOFF signal

When the synchrotron is functioning normally the ISIS_ON pulses are used to reset the counter 2CT_A3 every 20ms. This counter is continuously clocked by the 10kHz signal

R_CLK and if the period time of the ISIS pulses remains at 20ms then the counter simply counts to 200 (200×0.1ms=20ms) and is then reset. If however a failure does occur with the synchrotron then one or more of the ISIS pulses will be missing and so the counter 2CT.A3 will continue being incremented until it reaches a count of 300. Before a count of 201 is reached i.e. 1ms after the expected arrival time of the ISIS pulse the comparator subsystem will have produced the GRST signal and the watchdog system will have produced the W_DOG signal which are used to reset the TRS system. In system control their action is to reset 2FF.C6 and replace the enable on 2CT.A3 when 2FF.C6 is reset. The action of resetting 2FF.C6 removes the enable from 2FF.C5 and gate 2AD.D6b putting system control in the state described at the beginning of the last section. This means that once the ISIS pulses reappear then the first action of system control will be to produce the LOAD_LL and L_CLK signals for the limit generator.

Once the value in counter 2CT.A3 which is present at the B input of comparator 2CP.B3 is equal the value of 300 stored in the force component 2FR.B3 then this will cause the A_LE_B output of 2CP.B3 to go high producing the IOFF signal. This signal is sent to the watchdog circuit to produce the WDOG_B signal which in system control is used to disable the top gate in grid B7. In the watchdog circuit the WDOG_B signal is used to enable a counter that will, once the ISIS pulses return, count for 10 ISIS pulses before the WDOG_B signal is released. While the ISIS pulses are being monitored in this way the WDOG_B signal is used to prevent to production of superframes by inhibiting the gate in grid B7. The WDOG_B signal is used to keep 2CT.A3 enabled so should the ISIS neutron source fail again before the watchdog circuit has counted 10 consecutive ISIS pulses then comparator 2CP.B3 will issue another IOFF signal which will reset the counter in the watchdog circuit thereby restarting the count from zero.

A.4 Limit Generator System

The limit generator system (figure 19) is responsible for producing the limit window which is used to check the period time of all of the ISIS pulses within a superframe. The limit generator system is only used in the superframe mode and it is switched off when the superperiod mode is chosen. The data that controls the width of the limit window and its relative position with respect to the ISIS pulses is obtained from the main 16 bit data bus DATA_TR and this data is stored in register 2166 (3RG.B7). The limit window data is loaded into the register when the WRITE_LIM signal line becomes active as described in section A.2.

The first 8 bits (7:0) of the 16 bit data bus LIM_MAIN (Q_OUT of register '2166') contains the data that is responsible for positioning of the LL pulse (the start of the limit window) with respect to the ISIS pulse. This data is directed to the lower limit circuit (top half of schematic) via the data bus LIM_DATA_ONE and slice 3SL.B7a. The last 8 bits (15:8) contain the data for the position of the UL pulse, with respect to the start of the LL pulse, and this data is sent to the upper limit circuit (bottom half of schematic) via the data bus LIM_DATA_FIV and slice 3SL.B7b. The action of each circuit will be considered separately. The next section describes the operation of the lower limit circuit and section A.4.2 that of the upper limit circuit. Section A.4.3 looks at how the frequency of the two limit pulses are matched to the frequency of the ISIS pulses.

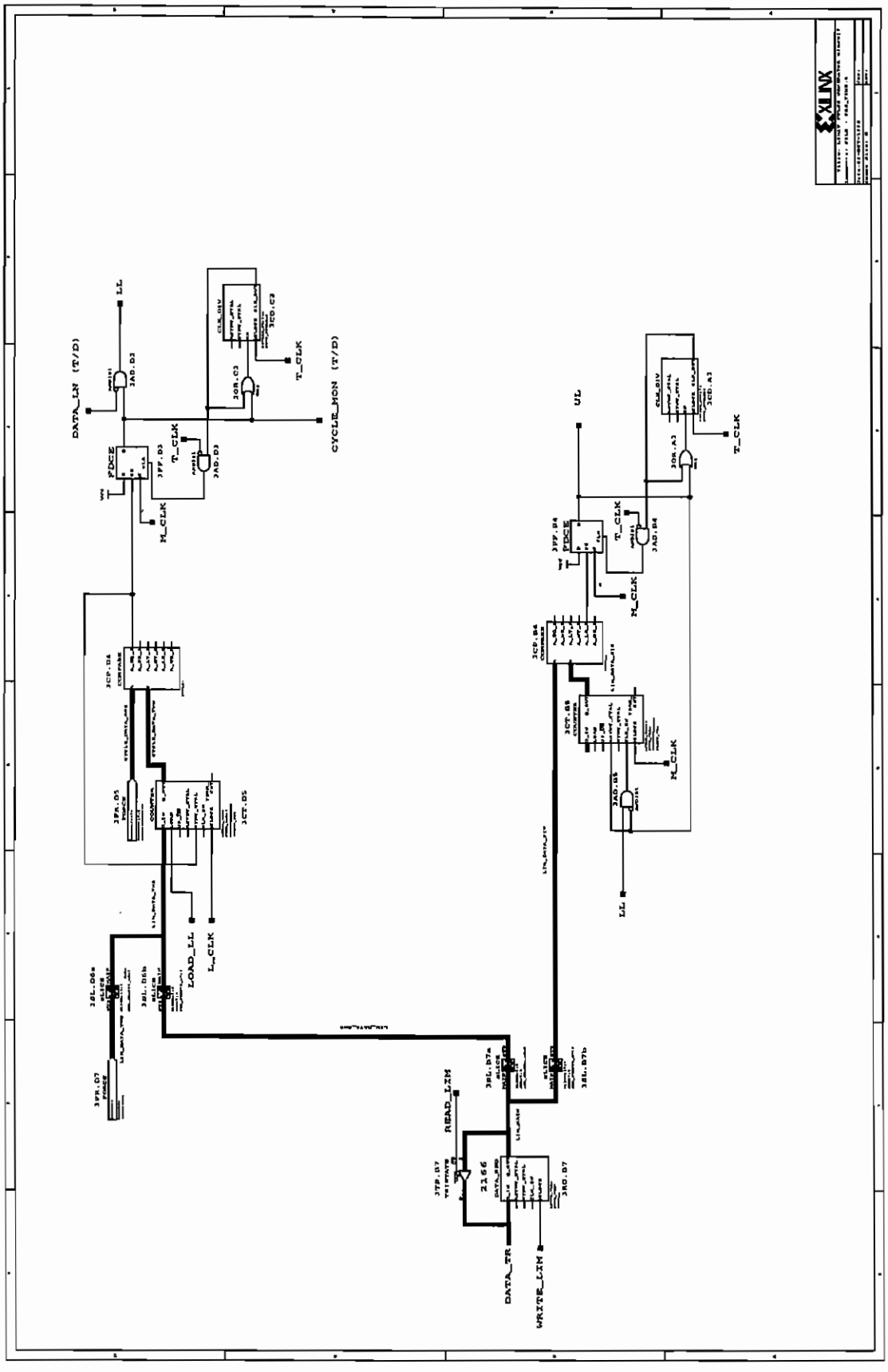

Figure 19: Xilinx schematic 4 - The limit generator system

A.4.1 The Lower Limit Circuit

The 8 bit data bus LIM_DATA_ONE emerges from slice 3SL.D6b as part of the 17 bit data bus LIM_DATA_THR. The other 9 bits of this data bus, all zeros, come from the force component 3FR.D7 via the data bus LIM_DATA_TWO and slice 3SL.D6a. This data on bus LIM_DATA_THR is fed to the D_IN input of counter 3CT.D5.

The limit generator circuit is initiated by the clock signal, L_CLK, which is gated out of system control (section A.3) when system controls receives the first ISIS pulse of the superframe. Before this happens however the counter 3CT.D5 will have been preloaded with the data on bus LIM_DATA_THR by the action of the previous ISIS pulse. This 'first' ISIS pulse causes system control to place a logic 1 on the LOAD_LL line which goes to the LOAD input of 3CT.D5 and also causes system control to activate the L_CLK line. Both of these actions last for 10μs. With the LOAD input of 3CT.D5 enabled the action of the L_CLK signal loads in the data at the D_IN input of the counter and this data will subsequently then appear on the bus, CYCLE_DATA_TWO, at the Q_OUT output of the counter and consequently the B input of the comparator 3CP.D4.

Once this initial load cycle is complete the limit generator does nothing else until the first ISIS pulse of the superframe is received which will activate the L_CLK line out of system control. When activated, the 5MHz L_CLK, signal will be used to increment the counter 3CT.D5 every 0.2μs thereby adding to the data already stored in the counter which was placed there during the initial load cycle. The output of 3CT.D5 in compared in the comparator (B input) against the data present at the A input of the comparator 3CP.D4. The data at the A input of this comparator is fixed by the force component 3FR.D5 which holds the value decimal 100000 (see section A.4.3). When the comparator inputs A and B become equal the A_EQ_B output of 3CP.D4 enables flip-flop 3FF.D3 which when clocked by M_CLK (within 0.1μs) will initiate the LL pulse via 3AD.D3. The other input to gate 3AD.D3 is always low except under certain test conditions.

The time between the first L_CLK pulse being received by the counter 3CT.D5 to the point where the A_EQ_B output of 3CP.D4 goes high (producing the LL pulse) is calculated to be 100,000$\times$0.2μs (=20ms) less the value that was preloaded into the D_IN input of the counter 3CT.D5. This means in effect that the action of preloading the counter allows the start of first LL pulse to appear before the expected arrival time of the second ISIS pulse. For example if the data at D_IN of 3CT.D5 was 25 decimal then the first LL pulse would appear at 5μs (25$\times$0.2μs) before the expected arrival time of the next ISIS pulse thereby forming the beginning of the limit window.

The LL signal will remain high until 3FF.D3 is reset by the action of 3AD.D3, 3OR.C3 and 3CD.C2. The clock divider 3CD.C2 is activated by the Q output of 3FF.D3 (i.e. the LL pulse) via 3OR.C3 which places a logic 1 on the enable (EN) input of 3CD.C2. Once enabled CLK_DIV 3CD.C2 (divide by 104, duty cycle=4) produces a 4μs pulse after an initial period of 100μs. The 4μs pulse resets 3FF.D3 by enabling gate 3AD.D3 which allows T_CLK through to the clear line of the flip-flop thereby ending the LL pulse after a time of 100μs. The 4μs pulse from the CLK_DIV is also fed to its own enable input via 3OR.C3 to replace the enable lost from flip-flop 3FF.D3 when it is reset. The clock divider will remain active until the end of its 4μs duty cycle when the loss of the 4μs pulse removes the enable thereby inhibiting the action of T_CLK at the clock input of 3CD.C2.

The A_EQ_B output of comparator 3CP.D4 is also fed to the SYNC_CTRL input of counter 3CT.D5 so that the next L_CLK pulse (e.g. pulse number 100001) will set the

counter to the value 1 (sync value=1 for this counter). This action establishes the count sequence ...99998, 99999, 100000, 1, 2 .. etc. The count sequence ensures that the next and all subsequent LL pulses will be at 20ms intervals (in line with the periodic time of the ISIS pulses) and keeping therefore at the same predetermined time before each ISIS pulse. The LL clock cycle will run until the penultimate ISIS pulse of the superframe has been received by the TRS system when the L_CLK line becomes deactivated by the action of the PRE_SF signal (section A.6) thereby stopping the cycle. However the L_CLK line will then be momentarily reactivated (together with LOAD_LL) for 10μs to initiate the preload sequence for counter 3CT.D5 ready for the start of the next superframe.

A.4.2 The Upper Limit Circuit

It is the LL pulse that initiates the production of the UL pulse. The LL pulse enables gate 3AD.B5 which places an enable on the CLK_EN input of counter 3CT.B5. The other input of gate 3AD.B5 (the UL line) is zero at this time. With the counter 3CT.B5 enabled the 10MHz clock signal M_CLK will start to increment the counter in 0.1μs intervals. The contents of 3CT.B5 will be present at the B input of the comparator 3CP.B4. The data at the A input of the comparator is that data received from the instrument computer which will have been chosen to give the required delay time (in 0.1μs units) from the first appearance of the LL pulse to the subsequent appearance of the leading edge of the UL pulse. When the A and B inputs of the comparator are equal the A_LE_B output of 3CP.B4 will enable flip-flop 3FF.B4 which is then set by the action of M_CLK producing the start of the UL signal. The UL signal disables the gate 3AD.B5 removing the CLK_EN signal to the counter 3CT.B5 and it also resets the counter to zero via its ASYNC_CTRL input. The action of 3AD.B4, 3OR.A3 and clock divider 3CD.A3 (divide by 154, duty cycle=4) resets 3FF.B4 after a period of 150μs by producing a 4μs pulse from the clock divider after a 150μs delay from the receipt of the first T_CLK pulse into 3CD.A3. This is the same procedure as described for the lower limit circuit. The 4μs pulse from 3CD.A3 enables gate 3AD.B4 which allows through T_CLK to the CLR line of 3FF.B4. The UL circuit is now completely reset and ready to receive the next LL pulse.

A.4.3 Frequency of the Limit Pulses

The frequency of the LL and UL pulse trains should be set at 50Hz (in line with ISIS) giving a periodic time between pulses of 20000μs. However checks carried out at ISIS over a period of 7 days (from 13th to the 20th September 1996) showed that the actual periodic time between the ISIS pulses as measured by a standard frequency counter was 19999.80$\pm$0.02μs. To bring the frequency of of the limit generator in line with that of ISIS the force component 3FR.D5 is set at 99999 ($\times$0.2μs=19999.80μs) rather than the nominal value of 100000.

A.5 The Comparator System

The function of the comparator system (figure 20) is to check the periodic time of the ISIS pulse train that makes up a single superframe to ensure that it remains at 20000μs, $\pm$ a small allowable error in the range 25.6μs as set by the limit generator circuit (see section A.4).

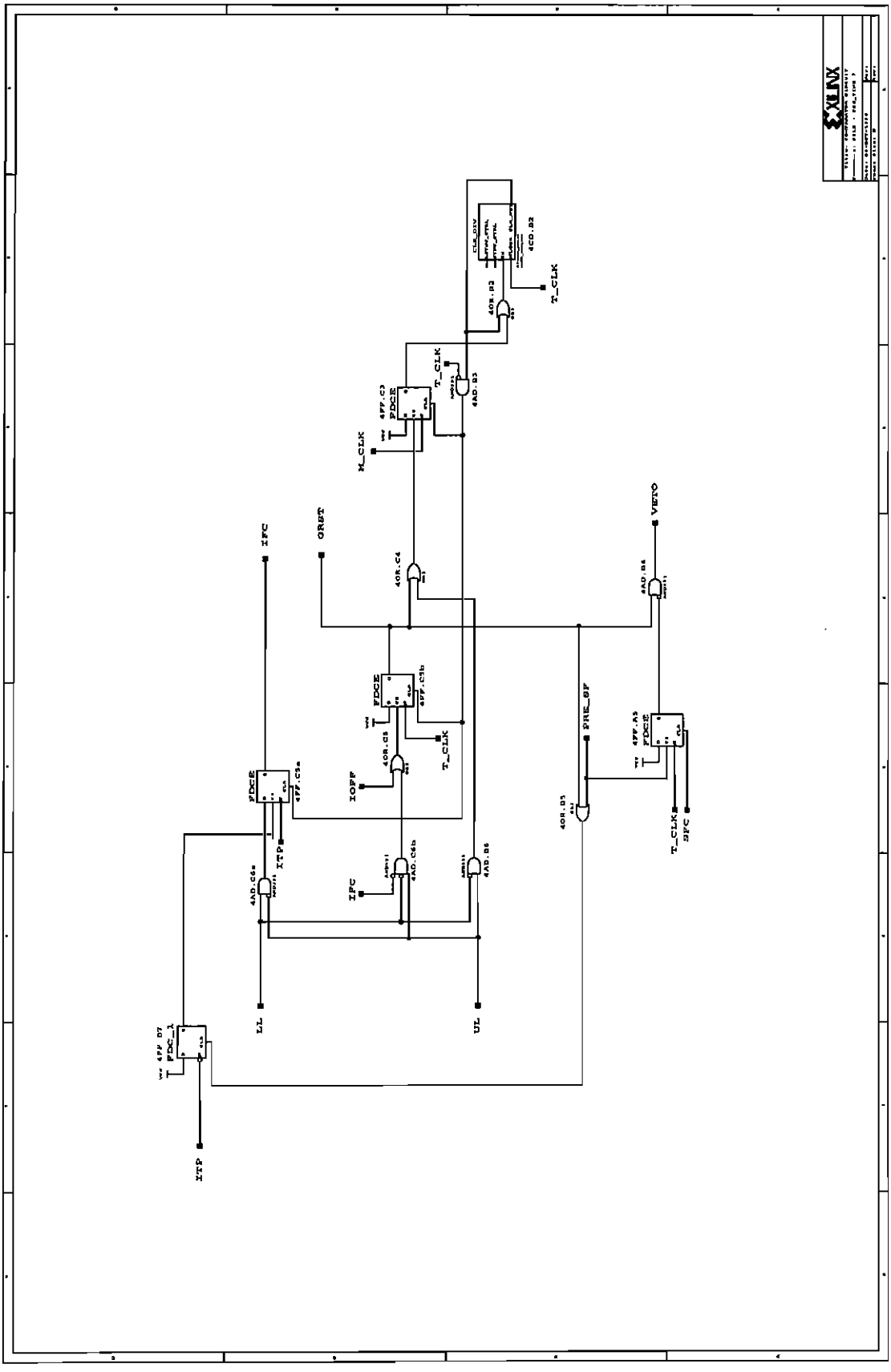

Figure 20: Xilinx schematic 5 - The comparator circuit

The main inputs to the comparator system are the ITP pulses, the gated ISIS pulses from system control, and the two limit pulses, the Lower Limit (LL) pulse of 100μs duration and the Upper Limit (UL) pulse of 150μs duration which form the limit window as described in section A.4. If all the ISIS (ITP) pulses lie within the limit window formed by the leading edges of the LL and UL pulses then a 'go' decision is made by the comparator system in the form of an IFC pulse. These IFC pulses are used within the superframe register to create the superframes of the required duration as described in section A.6. If any of the ITP pulses lie outside the limit window then a 'fail' decision results that takes the form of the (90μs) GRST and VETO pulses whose task it is to reset the TRS system and instruct the instruments DAE electronics to ignore all data collected during the superframe when the failure occurred.

A.5.1 Operation - Superframe Pass

The ITP pulses enter the comparator system at two places, the inverted clock input of flip-flop 4FF.D7 and the clock input of 4FF.C5a. The leading edge of the first ITP pulse to enter the system does not trigger 4FF.C5a because of the low signal on its clock enable input which stays low until the trailing edge of the first ITP pulse sets flip-flop 4FF.D7. The purpose of the first ITP pulse received by the comparator is just to 'switch on' this system (4FF.D7 effectively being the 'on switch') thereby preparing the comparator system to receive the LL and UL limit pulses from the limit generator which will also be activated by this first ISIS pulse.

After approximately 20ms after the first ISIS pulse has been received (and just before the next one appears) the first of the 100μs LL pulses will arrive from the limit generator system. This LL pulse will appear at the output of gate 4AD.C6a since the UL line is low at this time which enables gate 4AD.C6a, and the LL pulse will place a logic 1 at the D input of 4FF.C5a. Also the absence of the UL signal will ensure that the gates 4AD.C6b and 4AD.B6 will be disabled at this time. Before the first UL pulse arrives at the comparator (up to a maximum of 25.6μs after the LL pulse) an ITP pulse should arrive at the clock input of 4FF.C5a. Since the D input and clock enable of 4FF.C5a are now both high this ITP pulse will set 4FF.C5a thereby producing the start of the ($\sim$ 170μs) IFC pulse; a comparator 'pass' decision. The IFC signal also places a disable on gate 4AD.C6b whose function when enabled is to produce the GRST and VETO (fail) signals as will be described later. Following the appearance of the ITP pulse, the 150μs UL pulse will arrive from the limit generator and this pulse will place an enable on gate 4AD.B6 and 4AD.C6b although this second gate is disabled by the IFC signal as already mentioned. At the end of the LL pulse (UL still high), the output of gate 4AD.B6 places a clock enable on flip-flop 4FF.C3 via 4OR.C4. The Q output of 4FF.C3 will be clocked high (within 0.1μs) by the action of the 10MHz clock, M_CLK, and (90μs) after this has occurred the action of 4AD.B3, 4OR.B2 and clock divider 4CD.B2 (divide by 90, duty cycle 4) will enable gate 4AD.B3 for 4μs following a delay period of 90μs from receipt of the first T_CLK pulse into 4CD.B2. This action will allow T_CLK to be gated through 4AD.B3 for 4μs to reset 4FF.C3, 4FF.C5a and 4FF.C5b although this last flip-flop should already be reset at this time.

The resetting of 4FF.C5a completes the IFC pulse after a time of between 165-188μs depending on the size of the limit window which has a range of 2 to 25μs. With flip-flop 4FF.D7 remaining set, the above procedure is repeated for all ISIS (ITP) pulses within

the superframe. When the penultimate ISIS pulse of the superframe (as determined by the IFC counter in the superframe register) has been received by the TRS system the superframe register produces a PRE_SF pulse which resets 4FF.D7 via 4OR.B5 effectively switching off the comparator. The PRE_SF pulse also enables 4FF.A5 which is then set by T_CLK disabling gate 4AD.B4. This ensures that a VETO signal cannot be produced for this superframe if the synchrotron should fail at this point since now the superframe can be considered complete and therefore the data should be saved and not rejected.

A.5.2 Operation - Superframe Fail

If the ITP pulse arrives early i.e. before the LL pulse, then the D input of 4FF.C5a will be low when the clock input is triggered by the ITP pulse and so this flip-flop will remain effectively reset leaving an enable on gate 4AD.C6b. No IFC 'pass' signal can now be produced. The LL pulse will end with the (longer) UL pulse still active and this condition, together with the low Q output of 4FF.C5a, will ensure that the output of gate 4AD.C6b is high which will place an enable on flip-flop 4FF.C5b (via 4OR.C5) which will then be clocked within 1μs by T_CLK providing the start of the 90μs GRST (fail) signal. The GRST signal enables 4FF.C3 (via 4OR.C4) which is then set by M_CLK and as before T_CLK will appear at the output of 4AD.B3 for 4μs following a 90μs delay caused by the action of 4AD.B3, 4OR.B2 and 4CD.B2 which will reset 4FF.C5b thereby completing the GRST pulse. The GRST pulse is used to reset the TRS system and its action elsewhere is described in the relevant sections. Within the comparator system the GRST pulse is used to reset the comparators 'on switch', 4FF.D7, via 4OR.B5 thereby switching off the comparator system in the same manner as for the PRE_SF pulse. The GRST pulse is also passed through 4AD.B4 as the VETO signal which is then sent to the instruments DAE electronics to reject the data collected during the superframe.

If an ITP pulse was to arrive after the UL pulse has been produced then the same conditions apply as per an early pulse since its the arrival of the UL pulse together with the fact that 4FF.C5a is reset that triggers the production of the VETO pulse. An ISIS pulse arriving after the UL pulse has therefore no real effect since the reset cycle would have already been started.

A.5.3 Synchrotron Failure

Finally, if ISIS was to fail during a superframe then the situation would be the same as for a late or a early ITP pulse with the action of the limit pulses providing the required GRST and VETO pulses. However if ISIS fails after the penultimate ISIS pulse of the superframe has been received, then the comparator system would not be able to detect this since the limit generator and comparator systems are disabled at this point. In this situation system control (section A.3) will produce an IOFF signal 30ms after the last ISIS pulse was received by system control. In the comparator, the IOFF signal will set 4FF.C5b (clocked by T_CLK), producing the GRST signal as before. However in this case the data of the last superframe will not be lost since the VETO signal is not produced because 4AD.B4 is disabled by the output of 4FF.A5 which is set by the action of the PRE_SF signal (and T_CLK).

The last event to occur within the comparator following a synchrotron failure is the resetting of flip-flop 4FF.A5. Following the failure of the ISIS neutron source a series of

2 dummy superframes are produced by the superframe register before the TRS system switches to normal operation. This dummy run produces a SFC pulse at the end of the first dummy superframe and this SFC pulse is used here to reset 4FF.A5 at which stage the comparator system will now be in a fully reset condition, effectively switched off, awaiting the next ITP pulse which will indicate the end of the second dummy superframe and the start of the normal superframe cycle. This ITP pulse and will then set 4FF.D7 switching the comparator back on so it is ready to receive the LL, UL and ITP pulses 20ms later.

A.6 The Superframe Register

A full schematic of the superframe register is given in figure 21. The function of the superframe register is to form the superframe by allowing certain ISIS pulses to be gated straight to the instruments DAE and then blocking a set number of following ISIS pulses. The superframe register also provides the F2P_RST pulse if a failure occurs with the neutron source when the TRS system is running in the superperiod mode.

A.6.1 Operation - Superframe Mode

The operation of the superframe register will be considered from the point where a new superframe is about to be created i.e. an ISIS pulse is about to be gated through the TRS system to the instruments DAE. At this point the superframe register is reset with the exception of flip-flop 5FF.C5 which was set by the action of the last IFC pulse from the last superframe. The following text will explain how a complete superframe is produced from the superframe register.

With the superframe register in the state described above the next ISIS_INT pulse to be gated out of system control will enter the superframe register as shown on the left hand side of figure 21. This pulse is directed to the inputs of three gates, gates 5AD.C6, 5AD.B4b and 5AD.B4a. The gate 5AD.C6 is disabled at this point by the (high) output of 5FF.C5. Also another input to gate 5AD.C6, the DATA_LO signal line is low which also acts to disable this gate. The DATA_LO line is used to switch off the limit generator and the comparator systems and If selected causes the superframe register to operate is a slightly different way. This situation is discussed in section A.6.4. The second gate that the ISIS_INT pulse is sent to is gate 5AD.B4b. This gate is also disabled since the signal line on its other input, DATA_SM is low. This second input is an option offered by the superframe register which allows superframes equal to one ISIS frame to be produced. This feature is also discussed in section A.6.4 and for now it will be considered that only superframes made up of 2 or more ISIS frames are required. The third gate which receives the ISIS_INT pulse is gate 5AD.B4a. This gate is enabled by the Q output of 5FF.C5 and so the ISIS_INT pulse is gated through to 5AD.B3 via 5OR.B4a. If for now it is assumed that the synchrotron is running normally then the WDOG_A line that goes to the other input of 5AD.B3 will not be active which ensures that the gate 5AD.B3 is enabled. This situation allows the ISIS_INT pulse to pass through to gate 5AD.B2. This gate will be enabled since the DATA_SR signal line on its other input is low. This line is only active when the TRS system is running in the superperiod mode. This is discussed in section A.6.3. The ISIS_INT pulse can now leave the superframe register (and the TRS system) via 5OR.C2a and 5OR.C2b where it is sent to the instruments DAE to mark the

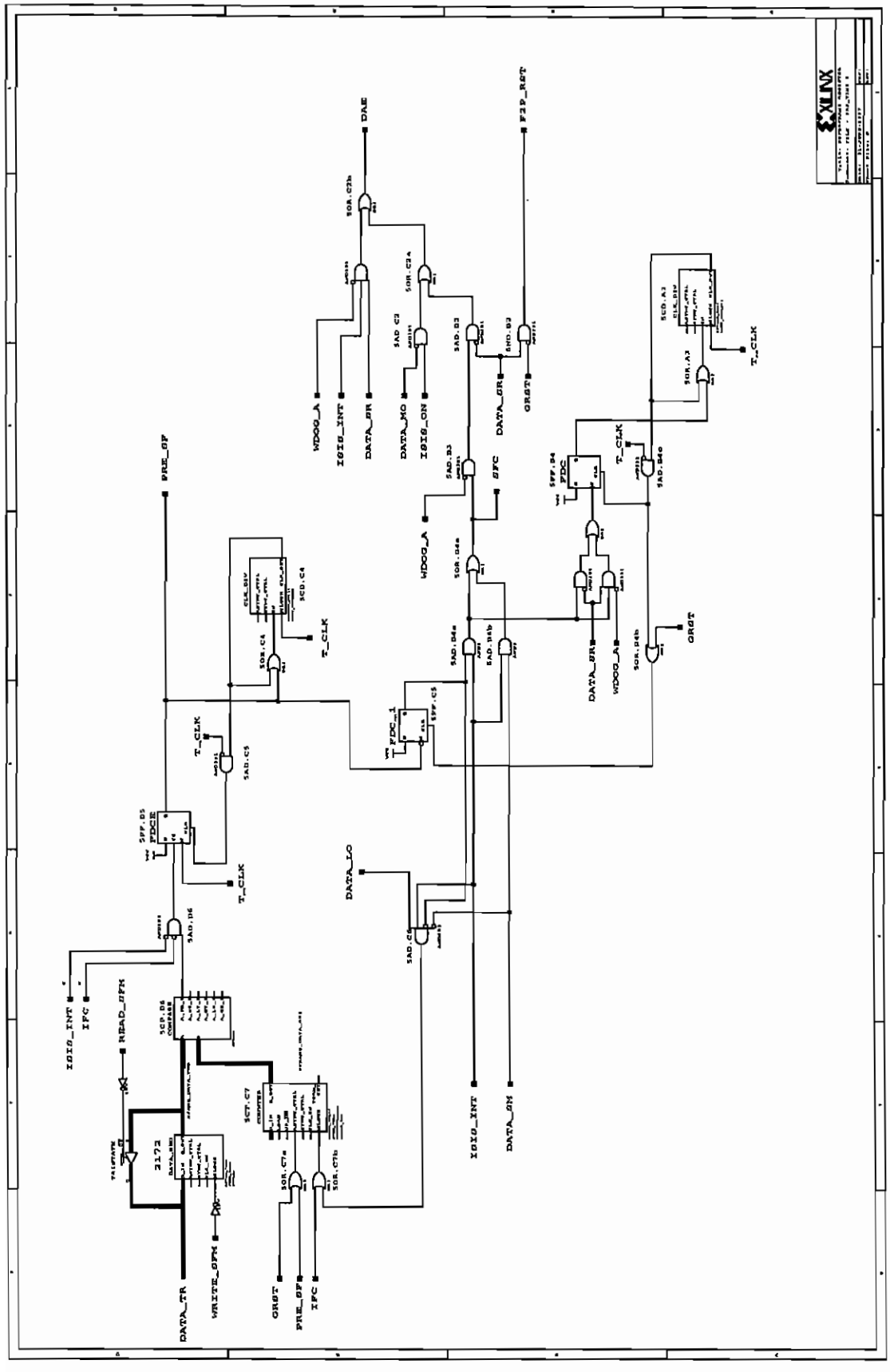

Figure 21: Xilinx schematic 6 - The superframe register

start of a superframe.

In addition to starting a superframe this ISIS_INT pulse is also used to trigger the electric field control system to produce the EFA pulse. This is done using the output of 5OR.B4a which is not only part of the path for the ISIS_INT pulses to the DAE but its output is also connected to the SFC input line of the electric field control system. It is therefore this first ISIS_INT pulse of the superframe, also relabelled as the SFC pulse, that initiates the production of the EFA pulse. This initial ISIS_INT pulse is also used to clock flip-flop 5FF.B4 via the enabled (top) AND gate in grid B4 (DATA_SR=0) and the OR gate on the clock input of 5FF.B4. The Q output of 5FF.B4 enables clock divider 5CD.A3 (divide by 8, duty cycle=4) which will produce a 4μs high signal after a period of 4μs from the time it was enabled. A high on the CLK_OUT output of 5CD.A3 will allow T_CLK to be gated through 5AD.B4c to reset flip-flop 5FF.B4 and 5FF.C5. Resetting 5FF.C5 disables gate 5AD.B4a thereby closing the route for the ISIS_INT pulses to the DAE.

When the next ISIS_INT pulse arrives from system control it will be ignored since all of its possible routes into the superframe register are now disabled. However this second ISIS_INT pulse would have also been sent to the comparator system where its arrival time (an indication of the periodic time of the ISIS pulses) would have been checked against the UL and LL pulses from the limit generator. If the ISIS_INT (=ITP pulse in comparator schematic) arrived in between the production of the LL and UL pulses then the comparator would have produced an IFC pulse which is sent to the clock input of 5CT.C7 via gate 5OR.C7b. This IFC pulse will increment the counter 5CT.C7 to 1 decimal and this count will appear at the B input of comparator 5CP.D6. The A input of 5CP.D6 comes from the data register 2172. This register is loaded with a decimal value that is equal to the number of ISIS frames within the superframe less 1. The superframe register now simply counts the IFC pulses as they are received from the comparator system. This will continue until the count at the Q_OUT bus output of 5CT.C7 is equal in size to the data stored in the register 2172. When this occurs the A_EQ_B output of 5CP.D6 goes high which places an enable on flip-flop 5FF.D5 which is then set by the action of the 1MHz T_CLK signal. The output of 5FF.D5 is the 10μs PRE_SF pulse which is produced by the action of the clock divider 5CD.C4 (divide by 14, duty period=4) and the gates 5OR.C4 and 5AD.C5. This set up works in the same way as perviously described for CLK_DIV 5CD.A3. The trailing edge of the PRE_SF pulse is used to set flip-flop 5FF.C5 thereby enabling once again gate 5AD.B4a which reestablishes the path for the ISIS_INT pulse to the instruments DAE. This allows the next ISIS_INT pulse to be gated out of the TRS system as the DAE pulse thereby starting a new superframe.

A.6.2 Reset Procedure - Superframes

In the event of a synchrotron failure a GRST pulse will be produced by the comparator system and a WDOG_A signal will also be produced from the watchdog system. The action of the GRST pulse is to reset the superframe counter 5CT.C7 to zero via 5OR.C7a. This must be done since the counter will be holding some non zero value corresponding to the number of IFC pulses that were received before the ISIS failure occurred. This value must be set to zero before any more superframes are started. The GRST pulse also resets flip-flop 5FF.C5 thus removing the path for the ISIS_INT pulses to the DAE.

Once the synchrotron is functioning normally again the superframe register will start to

receive ISIS_INT pulses once more. The superframe register will now start the production of superframes as described in the last section except this time flip-flop 5FF.C5 will not be set. This means that a DAE pulse will not be sent to the DAE to mark the start of the superframe although the superframe register will still go through the actions of producing a superframe. This first superframe is the first of two dummy superframes that are produced to ensure that both the TRS system and the neutron source are working normally before the 'proper' superframes, which includes the external field trigger signal, are produced. The last ISIS_INT pulse of this first dummy superframe will still create the PRE_SF pulse which will set flip-flop 5FF.C5 which in turn enables gate 5AD.B4a. This means that the next ISIS_INT pulse to be received by the superframe register (the first ISIS_INT pulse of the next superframe) is now gated through 5AD.B4a and 5OR.B4a to one input of 5AD.B3. This time gate 5AD.B3 is not enabled due to the action of the WDOG_A signal which was driven high when the neutron source failure occurred. Instead the ISIS_INT pulse is sent to the watchdog circuit via the SFC signal line where it is used to remove the WDOG_A signal. This action signals the start of the second dummy superframe. At the end of this second dummy superframe the PRE_SF signal is produced again. The superframe register is now in the state described at the beginning of the last section, i.e. the superframe register is reset with the exception of the flip-flop 5FF.C5.

A.6.3 Operation - Superperiod Mode

The superperiod mode of operation is selected by programming register 2164 in the data and register control circuit (section A.2) which sets the DATA_SR line high. In this mode the superframe register works in very much the same way as it does in the superframe mode with the exception that here the superframe pulses are not sent to the DAE but instead the DAE receives the 50Hz ISIS_INT pulses. These pulses are gated directly to the DAE when the DATA_SR line is active high which enables the AND gate in grid C2.

The DATA_SR line also enables 5ND.B2 so if the TRS system is reset at any time i.e. if there is a failure with the neutron source, an inverted GRST pulse will be sent to the DAE as the F2P_RST pulse to rest the 8 bit period counter in the DAE.

A.6.4 Special Functions

It is possible to run the TRS system without the limit generator functioning and in this situation the superframe register will not receive any IFC pulses to increment the superframe counter. To get around this problem the DATA_LO line is used (part of register 2164) which when active will enable gate 5AD.C6. The other inputs to this gate apart from the ISIS_INT pulses are from the Q output of 5FF.C5, which will be considered low to start with as in the previous section, and the DATA_SM line. The DATA_SM line is another special feature which will be dealt with separately and will be considered low at present.

The above set of condition means that the gate 5AD.C6 will be enabled allowing the ISIS_INT pulses to directly increment the superframe register in place of the IFC pulses. The procedure is now much the same as before except it should be noted that when the flip-flop 5FF.C5 is set then gate 5AD.C6 is disabled so that the next ISIS_INT pulse will go on as before to produce a DAE pulse but it will not be able to get to counter 5CT.C7

since this has been reset by the PRE_SF pulse to zero ready for the production of the next superframe. If the ISIS_INT pulse were to get through then the next and all subsequent superframes would be short by one ISIS frame.

The DATA_SM line is used when the length of the superframe required is only one ISIS frame long. In this case the superframe counter is not required and this line being active will disable 5AD.C6 preventing the ISIS_INT pulses reaching counter 5CT.C7. This DATA_SM line is also fed to system control where it prevents the production of the IFC clock pulses to 5CT.C7. With the DATA_SM line active gate 5AD.B4b is enabled allowing the ISIS_INT pulses to pass though 5OR.B4a and out as the SFC and (with WDOG_A low) the DAE pulses.

If the TRS system undergoes a reset condition for some reason then the action of the GRST signal resets the superframe counter via 5OR.C7a. It is also used to clear flip-flop 5FF.C5 thus ensuring that the superframe register is reset.

If it desired to override the TRS system then usually this done by setting register 2164 in the data and resister load system to zero which will cause the signal on the DATA_MO line to fall to zero, (the DATA_MO (Master Override) line is part of that register). This action will then prime gate 5AD.C2 which will allow the ISIS_ON (i.e. ISIS) pulses to pass unimpeded through 5AD.C2 and out of 5OR.C2b as DAE pulses.

A.7 External Field Control System

The external field control system is responsible for producing the EFA signal that is used to trigger the high voltage switching system described in section 4. A full schematic of this system is given in figure 22. The electric field control system consists of two circuits which are activated by the SFC pulse from the superframe register (section A.6). The SFC pulse is identical to the DAE pulse that is sent to the DAE electronics to mark the start (and end) of a superframe. One of the circuits, the delay circuit (top half of schematic), controls the delay time, in units of $10\mu s$, between the production of the SFC signal and the delayed production of the EFA signal. The lower circuit, the EFA length control circuit, determines the length of time for which the EFA signal is active, this can again can be controlled in $10\mu s$ units.

Section A.7.1 describes the delay circuit and section A.7.2 describes the action of the EFA length control circuit. Section A.7.3 details some of the control options available for this system.

A.7.1 External Field Delay Circuit

The SFC pulse from the superframe register enters the electric field control system at gate 6AD.C7 which is enabled under the following conditions. First the WDOG_A line must be inactive i.e. the TRS system is not under a reset condition and second the A_EQ_B outputs of comparators 6CP.C3 (NO_DLY signal) and 6CP.B3 (NO_LTH signal) must both be low. This is only true if registers 2168 and 2170 are loaded with a non zero value. This is because the counters 6CT.C4 and 6CT.B4 are reset at this stage which means that the A_EQ_B outputs of comparators 6CP.C3 and 6CP.B3 will then be zero. Hence, for the Electric Field system to operate both registers need to be loaded with non zero values.

From gate 6AD.C7, the SFC pulse follows two paths, one to gate 6AD.C6, and the

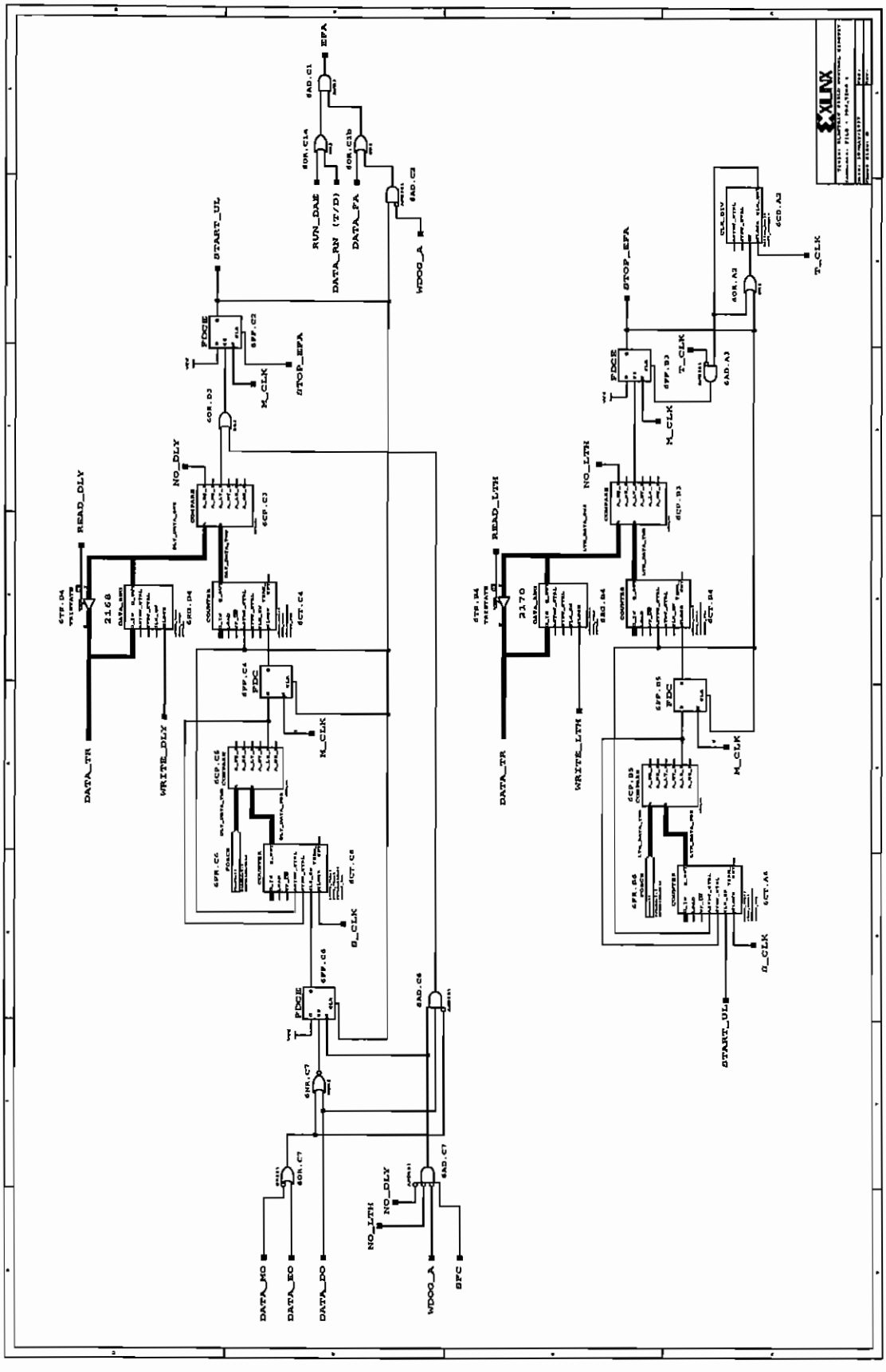

Figure 22: Xilinx schematic 7 - The external field control circuit

other path is to the clock input of 6FF.C6. The action of the SFC pulse is determined by the data lines DATA_MO, DATA_EO and DATA_DO. The data line DATA_MO carries the master override signal and is always set high under normal operating conditions. The DATA_EO line is used to inhibit the external field if required and the DATA_DO line is used to remove the delay between the SFC and the EFA pulses. These options are considered separately in section A.7.3 and for now both lines will be considered low. With the above conditions set the combination of 6OR.C7 and DATA_DO will place a clock enable on 6FF.C6 (via 6NR.C7) while the low on the DATA_DO line will inhibit gate 6AD.C6.

The clock enable on 6FF.C6 will allow an SFC pulse to set flip-flop 6FF.C6 which in turn will place a clock enable on counter 6CT.C6. This will allow the 5 MHz, S_CLK, to start incrementing the counter in steps of 0.2μs with the count value being recorded at the B input of 6CP.C5. The A input of 6CP.C5 comes from the force component 6FR.C6 which contains the value 50 decimal. Once the counter has reached 50 decimal the A_LE_B output of 6CP.C5 will place a logic 1 on the D input of 6FF.C4 and the SYNC_CTRL input of 6CT.C6.

Before the next S_CLK pulse arrives M_CLK (10 MHz) will set 6FF.C4. The rising edge of the signal on the Q output of 6FF.C4 will in turn increment counter 6CT.C4 by one count. The next S_CLK clock pulse will, due to the high now present on the SYNC_CTRL input set the counter 6CT.C6 to a value of 1 establishing the count sequence ...48, 49, 50, 1, 2...etc. This means that every 10μs (50$\times$0.2μs) counter 6CT.C4 will be incremented by 1. The output of counter 6CT.C4 is fed to the B input of comparator 6CP.C3 whose A input is connected to data register 2168.

Prior to the operation of the TRS system, data register 2168 will have been loaded with a value relating to the delay time required between the production of the SFC pulse and the subsequent production of the EFA signal, in units of 10μs. It should be noted that the minimum delay possible is 20μs (value of data in register 2168=1) since the A_LT_B output is used rather than the A_EQ_B output which is used only to control gate 6AD.C7. When the B input of 6CP.C3 is greater by one than the value contained in data register 2168 the A_LT_B output of 6CP.C3 will enable flip-flop 6FF.C2 via 6OR.D3. Within 0.1μs, through the action of M_CLK, the Q output of 6FF.D2 will go high producing the START_UL signal. The START_UL signal leaves the external field control system as the EFA signal via 6AD.C2, 6OR.C1b and 6AD.C1 under the two following conditions. The first condition is that the WDOG_A signal is not high and secondly that the gate 6AD.C1 has been primed by 6OR.C1a. The main input to 6OR.C1a is the RUN_DAE signal which is active when the instrument (for example PRISMA) commences a run. If the instrument is in its set up mode this line will be low and the EFA signal will therefore be inhibited. The other input to 6OR.C1a is the DATA_RN signal which can be used to replace the RUN_DAE signal for test/diagnostic purposes. Finally the other input to 6OR.C1b is the DATA_FA signal and this is used to establish a permanent EFA signal should this be required. This is achieved by setting the appropriate value in register 2164 as described in section A.2.

The START_UL signal is also sent to the ASYNC_CTRL input of 6CT.C4, the CLR inputs of 6FF.C4 and 6FF.C6 and the ASYNC_CTRL input of 6CT.C6 thus effectively resetting the delay circuit. Finally the START_UL signal places a clock enable on counter 6CT.A6 which starts the EFA length control circuit.

A.7.2 The EFA Length Control Circuit

This circuit works in much the same way to the delay circuit. The minor differences are that the A input of Comparator 6CP.B3 is fed from the data reg '2174' which will have been loaded with a value relating to the required length of the EFA signal again in 10μs.

When the required length of EFA signal has been reached the A_LT_B output of 6CP.B3 places an enable on 6FF.B3 whose Q output, the STOP_EFA signal, will reset 6FF.C2 ending the EFA signal. This action will also remove the enable from 6CT.A6 halting the 10μs cycle set up by 6CT.A6 and 6CP.B5. The STOP_EFA signal will also reset counters 6CT.B4 and 6CT.A6 via their ASYNC_CTRL inputs and will clear flip-flop 6FF.B4 completing the reset of the Length Control Circuit. The whole external field control system is now reset to its initial condition with the exception of 6FF.B3. However the 'high' output of 6FF.B3 also places an enable on clock divider 6CD.A2 (divide by 14, duty cycle=4). The output of 6CD.A2, via the action of 6AD.A3 and 6OR.A2, will remain zero for 10μs upon receipt of the enable signal and then will go high for 4μs. This will allow T_CLK to pass through 6AD.A3 for 4μs which will reset 6FF.B3. The electric field system is now ready for the next SFC pulse.

It should be noted that once started the electric field system will always produce the START_UL signal with the correct delay and length values as set up by the registers even if the TRS system is reset during its operation. Resetting the TRS system (WDOG_A signal high) will only prevent the START_UL signal leaving the external field system as the EFA signal it does not interfere with the production of the signal itself. The system will be allowed to finish and reset itself and then will wait for the next SFC pulse.

A.7.3 Control Options

The minimum delay offered by the delay circuit is 20μs so to get a delay of zero the DATA_DO line is used which like the DATA_EO and DATA_MO lines come from the output of Register 2164 (see section A.2). A high signal on the DATA_DO line disables 6FF.C6 putting the delay circuit offline. Instead this signal will enable gate 6AD.C6 which allows the SFC pulse to pass directly to the clock enable of 6FF.C2 via 6OR.D3 generating the START_UL (and hence EFA) signal as before.

The external field control system can be inhibited using the DATA_EO line which places an inhibit on 6AD.C6 and removes the clock enable from 6FF.C6. This is also true if the DATA_MO line is low. The DATA_MO line can be forced low when the TRS system is not required by loading register '2164' with zero.

A.7.4 EFA Delay and Length Step Size

It is the first counter/comparator combination of the delay and length circuits that controls the step size by which the delay and length of the EFA signal can be altered. The current value used in the force components 6FR.C6 and 6FR.B6 is 50 decimal giving a step size of 10μs (50$\times$0.2μs) although this value could be changed if required to give any required step size.

A possible modification to the external field control system would be to replace the force components with a data register thereby placing the step size under software control. For a 16 bit data bus where 8 bits are sent to the delay circuit and the other 8 bits to the length control circuit a range of programmable step sizes from 1μs (by loading the value

1285) up to 50μs (using 64250) would be possible allowing a maximum delay/length time of ~3.3s. This could be extended up to ~12 minutes if two 16 bit data registers were employed one feeding 6CP.C5 and the other 6CP.B5.

A.8 Watchdog System

The watchdog system (figure 23) is used to reset the TRS system in the event of a problem occurring with the neutron source. This problem could either be due to the ISIS frequency drifting so that the ISIS pulses arrive outside of the limit window set up by the limit generator, or there are no ISIS pulses present due to a complete failure of the synchrotron. The watchdog system consists of two circuits. The top circuit in figure 23 generates the WDOG_A signal if the frequency of the synchrotron drifts. In this event the WDOG_A signal, (together with the GRST signal from the comparator) is used to reset the TRS system and it has a special role of inhibiting the EFA signal from the external field control system. The lower circuit is responsible for producing the WDOG_B signal that puts the TRS system into its 'standby' if the synchrotron should completely fail. In the standby mode the TRS system will not immediately activate on receipt of the ISIS pulses but instead the watchdog system will be used to monitor the frequency of the ISIS pulses for 200ms to make sure the synchrotron is operating normally before it recommences superframe or superperiod production. These two circuits will be described separately in the following subsections starting with the upper, WDOG_A, circuit.

A.8.1 The WDOG_A Circuit

When a problem occurs during the construction of a superframe/superperiod as a result of a problem with the neutron source the comparator system (section A.5) will issue a GRST signal which is detected by the watchdog system. This GRST pulse sets flip-flop 7FF.D6 creating the start of the WDOG_A signal via 7OR.D4 which together with the GRST signal is used to reset the TRS system. The combination of these pulses will reset the superframe (IFC) counter, kill the EFA trigger signal from the electric field control circuit and switch off the limit generator and the comparator circuits. Following a TRS system reset it is system control (section A.3) that restarts the production of the superframes which it does by first producing two dummy superframes. After successful completion of the first dummy superframe, the superframe register (section A.6) produces the SFC signal which enters the watchdog system and via 7AD.D5 will clock flip-flop 7FF.D4. The Q output of 7FF.D4 reinforces the WDOG_A signal via 7OR.D4 and places an enable on clock divider 7CD.C3. The output of the clock divider (divide by 8, duty cycle 4) is a 4μs pulse after a 4μs delay from the time the clock divider was first enabled. The 4μs pulse places an enable on gate 7AD.C4 and becomes an hold on for its own enable input via 7OR.C4. With gate 7AD.C4 enabled, the signal on the other input of this gate, T_CLK, will be allowed through to reset 7FF.D6 and 7FF.D4 thereby removing the WDOG_A signal, the original enable to the clock divider. This is why the output of the clock divider is used as a second enable. This second enable allows 7CD.C3 to keep operating until it has produced the 4μs pulse at which time the enable is naturally removed and the clock divider is stopped at the beginning of its cycle.

It is important that the SFC pulse responsible for removing the WDOG_A signal does not also try to trigger the electric field control system since at this time no measurement

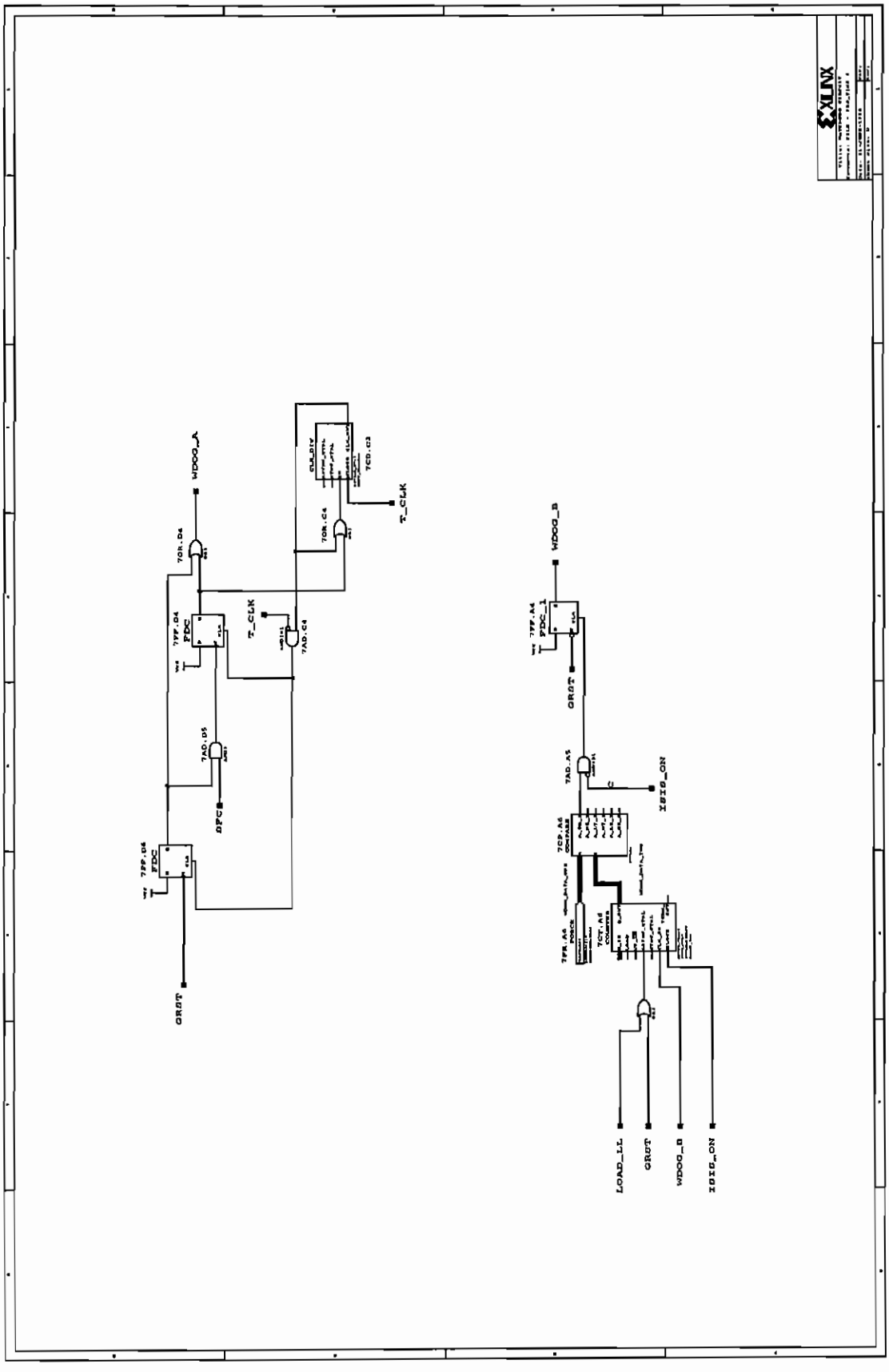

Figure 23: Xilinx schematic 8 - The watchdog system

is taking place. This is the reason why 7FF.D4 is used to reinforce the WDOG_A signal until the SFC pulse is finished.

A.8.2 The WDOG_B Circuit

Should the synchrotron completely fail an IOFF signal is produced by system control which causes the production of a GRST signal in the comparator system producing the WDOG_A signal as described above. At the end of the GRST pulse (90μs) the output of 7FF.A4 goes high producing the WDOG_B signal. This signal places an enable on counter 7CT.A6 and also inhibits the action of the ISIS pulses within system control (see section A.3) The TRS system is now in its standby mode and it cannot be restarted while the WDOG_B signal is high. When the synchrotron is functioning normally again the ISIS_ON (i.e. ISIS) pulses will be fed into the watchdog circuit where they are used to increment the now enabled counter, 7CT.A6. The counter will be incremented every time it receives an ISIS_ON pulse and the resulting count is sent to the B input of comparator 7CP.A6. The A input to the comparator is provided by the force component 7FR.A6 which has a nominal value of 10 decimal. If the ISIS pulse train continues uninterrupted, 7CT.A6 will continue to be incremented until it reaches a count of 10 decimal, equal to a time of 10×20ms=200ms, when the A_EQ_B output of 7CP.A6 will go high and reset flip-flop 7FF.A4 via 7AD.A5, but only at the end of the 400ns ISIS_ON pulse due to the second input on the gate 7AD.A5. The counter/comparator system 7CT.A6/7CP.A6 will produce a noise spike each time it is incremented by the ISIS_ON pulse. This noise spike is capable of resetting a flip-flop so to prevent this the output of the comparator is inhibited for 400ns by which time the output of the comparator is stable.

The loss of the WDOG_B signal removes the clock enable to 7CT.A6 and allows system control to resume the production of superframes which will include the production of the LOAD_LL signal which is used here as a reset (Q_OUT=0) for 7CT.A6, via gate 7OR.B6. If during the 8s count ISIS was to fail again another GRST signal would be produced resetting counter 7CT.A6 back to zero via the ASYNC_CTRL input. The counter would continue to be reset each time it received a GRST pulse until a continuous ISIS pulse train of 200ms duration was achieved and only then would the WDOG_B signal be removed.

B Programmes and Macros

In this appendix we list the FORTRAN programs and GENIE macros described in section(5).

B.1 The RUNTRS and OFFTRS Subroutines

```
      subroutine runtrs(ich,jlog)
      logical jlog
      common/files/in,iout,ismp,iang
      common/efield/eon,delay,durat,sfram,rlwin,ruwin
c---- get the values in registers 2164,2166,2168,2172,2174 in DAE ----
      jlog=.false.
      if(ich.eq.1) then
      ifail=0
      ireg=2164
      call getreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 100
      i2164=ival
      ireg=2166
      call getreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 100
      i2166=ival
      ireg=2168
      call getreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 100
      i2168=ival
      ireg=2170
      call getreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 100
      i2170=ival
      ireg=2172
      call getreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 100
      i2172=ival
c----- registers successfully read ---------------
c----- sfram = nos of superframes, use this to -----
c----- calculate the initial new value for register 2164 -------
      if(nint(sfram).gt.1) then
      if(nint(eon).ne.2) then
      j2164 = 1024
      else
      j2164 = 1024 + 64
      end if
      j2172 = (nint(sfram)-1)
      else
      j2164 = 33793
```

```
       end if
c----- now check the delay value --------------
       if(nint(delay).gt.9) then
       j2168 = nint(delay/10.) - 1
       else
       j2168 = i2168
       j2164 = j2164 + 4096
       end if
c----- now check the duration value ------------
       if(nint(eon).lt.0.or.nint(durat).lt.10) then
       j2170 = i2170
       if(nint(eon).eq.(-2)) then
       j2164 = j2164 + 512
       else
       j2164 = j2164 + 8192
       end if
       else
       j2170 = nint(durat/10.) - 1
       end if
c----- now the limit check on the intermediate frames -----
       if(nint(rlwin+ruwin).lt.1) then
       j2166 = i2166
       j2164 = j2164 + 16384
       else
       rlwin5=nint(rlwin*5.)/5.
       ruwin5=nint(ruwin*5.)/5.
       j2166 = 2565 * rlwin5 + 2560 * ruwin5
       end if
c----- Write the new values to the DAE register if they are ------
c----- different from the old values ----------------------------
       jfail = 0
       if(j2166.ne.i2166) then
       jreg = 2166
       jval = j2166
       call putreg(jfail,jreg,jval)
       if(jfail.ne.0) go to 150
       end if
       if(j2170.ne.i2170) then
       jreg = 2170
       jval = j2170
       call putreg(jfail,jreg,jval)
       if(jfail.ne.0) go to 150
       end if
       if(j2168.ne.i2168) then
       jreg = 2168
       jval = j2168
       call putreg(jfail,jreg,jval)
```

```
      if(jfail.ne.0) go to 150
      end if
      if(j2164.ne.i2164) then
      jreg = 2164
      jval = j2164
      call putreg(jfail,jreg,jval)
      if(jfail.ne.0) go to 150
      end if
      if(j2172.ne.i2172) then
      jreg = 2172
      jval = j2172
      call putreg(jfail,jreg,jval)
      if(jfail.ne.0) go to 150
      end if
c----- all registers successfully set to new values ------
      jlog=.true.
      return
      end if
      if(ich.eq.2) then
      ifail=0
      ireg=2164
      ival=0
      call putreg(ifail,ireg,ival)
      if(ifail.ne.0) go to 170
      return
      end if
c----- error messages --------
  100 continue
      write(iout,102)
  102 format(/,5x,'ERROR - ERROR : Occurred in subroutine RUNTRS')
      write(iout,101) ifail,'read from',ireg,ival
  101 format(/,5x,'Error code ',i5,' returned while trying to ',a,
     &' register ',i5,' value returned ',i5)
      write(iout,103)
  103 format(/,5x,'Aborting whole command')
      return
  150 continue
      write(iout,102)
      write(iout,101) jfail,'write to',jreg,jval
      write(iout,103)
      return
  170 continue
      write(iout,102)
      write(iout,101) ifail,'write to',ireg,ival
      write(iout,171)
  171 format(/,5x,'ERROR - ERROR : The time resolved circuit may ',
     &'not have been turned off')
```

```
        return
        end
c
c
        subroutine offtrs
        common/files/in,iout,ismp,iang
        dimension jreg(4)
c--- This subroutine is called to clear all time resolved circuit
c--- registers in the DAE.
        jreg(1)=2164
        jreg(2)=2166
        jreg(3)=2168
        jreg(4)=2174
        nreg=4
        do 1 i=1,nreg
        ival=0
        ifail=0
        ireg=jreg(i)
        call putreg(ifail,ireg,ival)
        if(ifail.ne.0) then
        write(iout,102)
  102   format(/,5x,'ERROR - ERROR : Occurred in subroutine OFFTRS')
        write(iout,101) ifail,ireg,ival
  101   format(/,5x,'Error code ',i5,' returned while trying to '
     &,'write to register ',i5,' value returned ',i5)
        end if
  1     continue
        return
        end
C
C
        SUBROUTINE GETREG(IFAIL,IREG,IIVAL)
        IMPLICIT NONE

        INCLUDE '($SYIDEF)'

C Declare variables and function return values
        INTEGER*4 SYS$TRNLOG,OPEN_DAE,CLOSE_DAE,WIO,RIO
        INTEGER*4 INST_LEN,IREG,IIVAL,STATUS,IFAIL
        INTEGER*4 IVAL,IO_CHANNEL
        CHARACTER*15 INST_NAME

C Before a any communictation is made to the DAE it has to be connected.
C The connection proocedure is as follows (with checks).

         STATUS=SYS$TRNLOG('INST_NAME',INST_LEN,INST_NAME,,,)
         IF (.NOT. STATUS) THEN
```

```
C         IFAIL=STATUS
          IFAIL=1
          RETURN
          END IF

          STATUS = OPEN_DAE(INST_NAME(:INST_LEN))
          IF (.NOT. STATUS) THEN
C         IFAIL=STATUS
          IFAIL=2
          RETURN
          END IF
IO_CHANNEL = 0
C DAE is now connected

C Talk to DAE
C Use functions WIO to write to DAE and RIO to read.
C paramiters: (INTEGER*4 address, INTEGER*2 data, INTEGER*4 io_channel)
C io_channel is not used for SCSI interface (was needed for QBus)
  STATUS = RIO(IREG, IVAL, IO_CHANNEL)
IF (.NOT. STATUS) THEN
C         IFAIL=STATUS
          IFAIL=4
          GO TO 2
          end if
          IIVAL=IVAL

C When communiction with the DAE is done and before the program finishes the
C DAE should be disconnected using the CLOSE_DAE function.
  2       CONTINUE
STATUS = CLOSE_DAE()
         RETURN
         END
C
C
         SUBROUTINE PUTREG(IFAIL,IREG,IIVAL)
         IMPLICIT NONE

         INCLUDE '($SYIDEF)'

C Declare variables and function return values
         INTEGER*4 SYS$TRNLOG,OPEN_DAE,CLOSE_DAE,WIO,RIO
         INTEGER*4 INST_LEN,IREG,IIVAL,STATUS,IFAIL
         INTEGER*4 IVAL,IO_CHANNEL
         CHARACTER*15 INST_NAME

C Before a any communictation is made to the DAE it has to be connected.
C The connection proocedure is as follows (with checks).
```

```
        IVAL=IIVAL

        STATUS=SYS$TRNLOG('INST_NAME',INST_LEN,INST_NAME,,,)
        IF (.NOT. STATUS) THEN
C        IFAIL=STATUS
        IFAIL=1
        RETURN
        END IF

        STATUS = OPEN_DAE(INST_NAME(:INST_LEN))
        IF (.NOT. STATUS) THEN
C       IFAIL=STATUS
        IFAIL=2
        RETURN
        END IF
IO_CHANNEL = 0
C DAE is now connected

C Talk to DAE
C Use functions WIO to write to DAE and RIO to read.
C paramiters: (INTEGER*4 address, INTEGER*2 data, INTEGER*4 io_channel)
C io_channel is not used for SCSI interface (was needed for QBus)
        STATUS = WIO( IREG, ival, IO_CHANNEL)
IF (.NOT. STATUS) THEN
C       IFAIL=STATUS
        IFAIL=3
        GO TO 2
        END IF

C When communiction with the DAE is done and before the program finishes the
C DAE should be disconnected using the CLOSE_DAE function.
  2     CONTINUE
STATUS = CLOSE_DAE()
RETURN
END
```

B.2 The HWRIT Program

```
      dimension iperio(256)
      in=5
      iout=6
      write(iout,10)
 10   format(/,5x,'Enter the nos of periods : ',$)
      read(in,*) nper
      write(iout,12)
 12   format(/,5x,'Enter the nos of frames per array element : ',$)
      read(in,*) nfpp
```

```
 15   continue
      write(iout,14)
 14   format(/,5x,'Enter nos of array elements (2,4,8,...) : ',$)
      read(in,*) narr
      do 16 i=1,9
      itwo_pow=2**(i-1)
      if(narr.eq.itwo_pow) go to 18
 16   continue
      write(iout,17)
 17   format(/,5x,'Must be a power of 2 from 1 to 256 ')
      go to 15
 18   continue
      write(iout,19)
 19   format(/,5x,'Enter the period for each array element : ')
      do 20 i=1,narr
 22   continue
      write(iout,21) i
 21   format(/,5x,'Element ',i3,' : ',$)
      read(in,*,err=22) iperio(i)
 20   continue
      open(unit=42,file='hardperiods.dat',status='unknown')
      write(42,*) nper
      write(42,*) nfpp
      nloop=256/narr
      do 1 i=1,nloop
      do 2 j=1,narr
      write(42,*) iperio(j)
 2    continue
 1    continue
      close(unit=42)
      write(iout,30) (nfpp*narr)
 30   format(/,5x,'The superframe length is ',i5)
      stop
      end
```

B.3 The TDD4 Macro

```
$ LABEL7:
$ INQUIRE IRUNN "ENTER THE RUN NUMBER :"
$ RLI=9.035
$ rlf1=0.8321
$ rlf2=0.8304
$ rlf3=0.8288
$ rlf4=0.8276
$ rlf5=0.8266
$ rlf6=0.8258
$ rlf7=0.8253
```

```
$ rlf8=0.8251
$ rlf9=0.8251
$ rlf10=0.8253
$ rlf11=0.8258
$ rlf12=0.8266
$ rlf13=0.8276
$ rlf14=0.8288
$ rlf15=0.8304
$ rlf16=0.8321
$ RLM1=-1.052
$ T0=4.0
> ASS 'IRUNN'
$ IRUN=0
$ INQUIRE NDET "ENTER THE NUMBER OF DETECTORS BEING COUNTED :"
$ INQUIRE MDET "ENTER THE ACTUAL DETECTOR NUMBER FOR ANALYSIS : "
$ INQUIRE ITYPE "ENTER NOS FOR X-UNITS (1)LAMDA (2)EI (3)D (4)ToF (5)Q :"
$ GOTO (XLAB1,XLAB2,XLAB3,XLAB4,XLAB5) ITYPE
$ XLAB1:
$ LTYPE="LAM"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB2:
$ LTYPE="E"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB3:
$ LTYPE="D"
$ GOTO QPHI
$ XLAB5:
$ LTYPE="Q"
$ QPHI:
$ INQUIRE PHI "ENTER THE ABSOLUTE PHI ANGLE IN DEGREES :"
$ XLAB4:
$ INQUIRE X_LO "ENTER THE MINIMUM X-VALUE :"
$ INQUIRE X_HI "ENTER THE MAXIMUM X-VALUE :"
$ INQUIRE X_STEP "ENTER THE X BIN SIZE :"
$ LABEL1:
$ INQUIRE NFRAM "ENTER THE SUPERFRAME NUMBER : "
$ ISHFT=-1*(NFRAM-1)*20000
$ INQUIRE IDET "ENTER THE DETECTOR SPECTRUM(1,..,'NDET')FOR ANALYSIS :"
$ INQUIRE IPT "ENTER THE POINT IN THE SCAN:"
$ LABEL3:
$ ISPCT=IDET+(NDET+3)*(IPT-1)
$ IMONT=NDET+1+(NDET+3)*(IPT-1)
$ IRUN=IRUN+1
> W'IRUN'=S'IMONT'
> TSHIFT 'ISHFT' W'IRUN'
```

```
> REBIN W'IRUN' 5:20000
> INT W'IRUN' 1000. 12000.
$ RMONT=100000./V1
> W'IRUN'=S'ISPCT'
> TSHIFT 'ISHFT' W'IRUN'
> REBIN W'IRUN' 5:20000
> TSHIFT 'T0' W'IRUN'
$ GOTO (XLAB7,XLAB7,XLAB7,XLAB8,XLAB7) ITYPE
$ XLAB7:
$ RLF=RLF'MDET'
> SET PAR W'IRUN' 'RLI' 'RLF' 'PHI' 0 10.
> U/'LTYPE' W'IRUN'
> W'IRUN'='RMONT'*W'IRUN'
$ XLAB8:
> REB W'IRUN' 'X_LO' ('X_STEP') 'X_HI'
> D/H W'IRUN' 'X_LO' 'X_HI'
!---------------------------------------------------------------
> INT W'IRUN' 'X_LO' 'X_HI'
!---------------------------------------------------------------
$ GOTO (XLAB9,XLAB9,XLAB9,XLAB6,XLAB9) ITYPE
$ XLAB9:
! WORKSPACE 'IRUN' CONTAINS SPECTRUM 'ISPCT' (IE POINT 'IPT') (MONITOR=100000)
$ GOTO YLAB1
$ XLAB6:
! WORKSPACE 'IRUN' CONTAINS SPECTRUM 'ISPCT' (IE POINT 'IPT')
$ YLAB1:
$ ICH=7
$ LABEL8:
!   OPTIONS ARE (1) EXIT, (2) DIFF DET/POINT/SFRAME, (3) DIFFERENT RUN
!               (4) K/H LAST PLOT, (5) PLASER7 LAST K/H, (6) FF LAST PLOT
$ INQUIRE ICH "ENTER 1,2,3,4,5,6 OR PRESS RETURN FOR NEXT POINT :"
$ GOTO (LABEL0,LABEL2,LABEL7,LABEL9,LABLL1,LABLL2,LABEL2) ICH
$ LABEL2:
$ IRUNT=IRUN/16
$ IRUNT=IRUNT+1
$ GOTO (LABEL4,LABEL5) IRUNT
$ LABEL5:
$ IRUN=0
$ LABEL4:
$ GOTO (LABEL0,LABEL1,LABEL6) ICH
$ LABEL6:
$ IPT=IPT+1
$ GOTO LABEL3
$ LABEL9:
> K/H
$ GOTO LABEL8
$ LABLL1:
```

```
> J "PLASER7 DEC_POSTSCRIPT.DAT"
$ GOTO LABEL8
$ LABLL2:
! ---------- NOT AVAILABLE AT THIS TIME ---------------------
$ GOTO LABEL8
$ LABEL0:
```

B.4 The ASF4 Macro

```
$ LABEL7:
$ INQUIRE IRUN1 "ENTER THE FIRST RUN NUMBER :"
$ INQUIRE IRUN2 "ENTER THE  LAST RUN NUMBER :"
$ NRUN=1+IRUN2-IRUN1
$ RLI=9.035
$ rlf1=0.8321
$ rlf2=0.8304
$ rlf3=0.8288
$ rlf4=0.8276
$ rlf5=0.8266
$ rlf6=0.8258
$ rlf7=0.8253
$ rlf8=0.8251
$ rlf9=0.8251
$ rlf10=0.8253
$ rlf11=0.8258
$ rlf12=0.8266
$ rlf13=0.8276
$ rlf14=0.8288
$ rlf15=0.8304
$ rlf16=0.8321
$ RLM1=-1.052
$ T0=4.0
$ INQUIRE NDET "ENTER THE NUMBER OF DETECTORS BEING COUNTED :"
$ INQUIRE MDET "ENTER THE ACTUAL DETECTOR NUMBER FOR ANALYSIS : "
$ INQUIRE ITYPE "ENTER NOS FOR X-UNITS (1)LAMDA (2)EI (3)D (4)ToF (5)Q :"
$ GOTO (XLAB1,XLAB2,XLAB3,XLAB4,XLAB5) ITYPE
$ XLAB1:
$ LTYPE="LAM"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB2:
$ LTYPE="E"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB3:
$ LTYPE="D"
$ GOTO QPHI
```

```
$ XLAB5:
$ LTYPE="Q"
$ QPHI:
$ INQUIRE PHI "ENTER THE ABSOLUTE PHI ANGLE IN DEGREES :"
$ XLAB4:
$ INQUIRE X_LO "ENTER THE MINIMUM X-VALUE :"
$ INQUIRE X_HI "ENTER THE MAXIMUM X-VALUE :"
$ INQUIRE X_STEP "ENTER THE X BIN SIZE :"
$ INQUIRE NFRAM "ENTER THE NOS OF SUPERFRAMES : "
$ INQUIRE IDET "ENTER THE DETECTOR SPECTRUM(1,..,'NDET')FOR ANALYSIS :"
$ INQUIRE IPT "ENTER THE POINT IN THE SCAN:"
$ DO IRUNN=IRUN1,IRUN2
> ASS 'IRUNN'
$ IRUN=1
$ ISPCT=IDET+(NDET+3)*(IPT-1)
$ IMONT=NDET+1+(NDET+3)*(IPT-1)
$ DO IFRAM=1,NFRAM
$ ISHFT=-1*(IFRAM-1)*20000
> W'IRUN'=S'IMONT'
> TSHIFT 'ISHFT' W'IRUN'
> REBIN W'IRUN' 5:20000
> TSHIFT 'T0' W'IRUN'
> INT W'IRUN' 1000. 12000.
$ RMONT=100000./V1
> W'IRUN'=S'ISPCT'
> TSHIFT 'ISHFT' W'IRUN'
> REBIN W'IRUN' 5:20000
> TSHIFT 'T0' W'IRUN'
$ GOTO (XLAB7,XLAB7,XLAB7,XLAB8,XLAB7) ITYPE
$ XLAB7:
$ RLF=RLF'MDET'
> SET PAR W'IRUN' 'RLI' 'RLF' 'PHI' 0 10.
> U/'LTYPE' W'IRUN'
> W'IRUN'='RMONT'*W'IRUN'
$ XLAB8:
> REB W'IRUN' 'X_LO' ('X_STEP') 'X_HI'
!-------------------------------------------------------------
> INT W'IRUN' 'X_LO' 'X_HI'
$ v3=ifram
$ v4=irunn
> fu w'irun' prisma_knh_gen:stofil w'irun'
!-------------------------------------------------------------
$ END DO
$ END DO
> J/R "PRISMA_KNH_GEN:TRSORT"
```

B.5 The ASP4 Macro

```
$ LABEL7:
$ INQUIRE IRUN1 "ENTER THE FIRST RUN NUMBER :"
$ INQUIRE IRUN2 "ENTER THE  LAST RUN NUMBER :"
$ NRUN=1+IRUN2-IRUN1
$ RLI=9.035
$ rlf1=0.8321
$ rlf2=0.8304
$ rlf3=0.8288
$ rlf4=0.8276
$ rlf5=0.8266
$ rlf6=0.8258
$ rlf7=0.8253
$ rlf8=0.8251
$ rlf9=0.8251
$ rlf10=0.8253
$ rlf11=0.8258
$ rlf12=0.8266
$ rlf13=0.8276
$ rlf14=0.8288
$ rlf15=0.8304
$ rlf16=0.8321
$ RLM1=-1.052
$ T0=4.0
$ INQUIRE NDET "ENTER THE NUMBER OF DETECTORS BEING COUNTED :"
$ INQUIRE MDET "ENTER THE ACTUAL DETECTOR NUMBER FOR ANALYSIS : "
$ INQUIRE ITYPE "ENTER NOS FOR X-UNITS (1)LAMDA (2)EI (3)D (4)ToF (5)Q :"
$ GOTO (XLAB1,XLAB2,XLAB3,XLAB4,XLAB5) ITYPE
$ XLAB1:
$ LTYPE="LAM"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB2:
$ LTYPE="E"
$ PHI=90.0
$ GOTO XLAB4
$ XLAB3:
$ LTYPE="D"
$ GOTO QPHI
$ XLAB5:
$ LTYPE="Q"
$ QPHI:
$ INQUIRE PHI "ENTER THE ABSOLUTE PHI ANGLE IN DEGREES :"
$ XLAB4:
$ INQUIRE X_LO "ENTER THE MINIMUM X-VALUE :"
$ INQUIRE X_HI "ENTER THE MAXIMUM X-VALUE :"
```

```
$ INQUIRE X_STEP "ENTER THE X BIN SIZE :"
$ INQUIRE NPT "ENTER THE NOS OF PERIODS : "
$ INQUIRE IDET "ENTER THE DETECTOR SPECTRUM(1,..,'NDET')FOR ANALYSIS :"
$ DO IRUNN=IRUN1,IRUN2
> ASS 'IRUNN'
$ IRUN=1
$ DO IPT=1,NPT
$ ISPCT=IDET+(NDET+3)*(IPT-1)
$ IMONT=NDET+1+(NDET+3)*(IPT-1)
> W'IRUN'=S'IMONT'
> REBIN W'IRUN' 5:20000
> TSHIFT 'T0' W'IRUN'
> INT W'IRUN' 1000. 12000.
$ RMONT=100000./V1
> W'IRUN'=S'ISPCT'
> REBIN W'IRUN' 5:20000
> TSHIFT 'T0' W'IRUN'
$ GOTO (XLAB7,XLAB7,XLAB7,XLAB8,XLAB7) ITYPE
$ XLAB7:
$ RLF=RLF'MDET'
> SET PAR W'IRUN' 'RLI' 'RLF' 'PHI' 0 10.
> U/'LTYPE' W'IRUN'
> W'IRUN'='RMONT'*W'IRUN'
$ XLAB8:
> REB W'IRUN' 'X_LO' ('X_STEP') 'X_HI'
!-------------------------------------------------------------
> INT W'IRUN' 'X_LO' 'X_HI'
$ v3=IPT
$ v4=irunn
> fu w'irun' prisma_knh_gen:stofil w'irun'
!-------------------------------------------------------------
$ END DO
$ END DO
> j/r "prisma_knh_gen:traver"
```

B.6 The STOFIL Program

```
      INCLUDE 'GENIE_SOURCES:FUNCTCOM.CMN'
      CALL FUNCTION_IN
      sumi=ST_VAR(1)
      erri=ST_VAR(2)
      ifram=nint(ST_VAR(3))
      irun=nint(ST_VAR(4))
      OPEN(UNIT=42,FILE='TRSTOR.DAT',ACCESS='APPEND'
     *,CARRIAGECONTROL='LIST',STATUS='UNKNOWN')
      WRITE(42,1) IRUN,IFRAM,SUMI,ERRI
1     FORMAT(3X,I6,3X,I3,3X,F7.2,3X,F7.2)
```

```
      CLOSE(UNIT=42)
      CALL FUNCTION_OUT
      STOP '            '
      END
```

B.7 The TRSORT Program

```
      DIMENSION IRUN(1000),IFRAM(1000),SUMI(1000),ERRI(1000),DEL(50)
      DIMENSION SUMJ(10),ERRJ(10)
      OPEN(UNIT=42,FILE='TRSTOR.DAT',STATUS='UNKNOWN')
      II=1
 99   CONTINUE
      READ(42,*,END=100) IRUN(II),IFRAM(II),SUMI(II),ERRI(II)
      II=II+1
      GO TO 99
 100  CONTINUE
      CLOSE(UNIT=42)
      II=II-1
      OPEN(UNIT=41,FILE='PRISMA_KNH_GEN:DELS.DAT',STATUS='old',
     &readonly)
      DO 1 I=1,24
      READ(41,*) DEL(I)
 1    CONTINUE
      CLOSE(UNIT=41)
      IMIN=100000
      DO 2 I=1,II
      IF(IRUN(I).LT.IMIN) IMIN=IRUN(I)
 2    CONTINUE
      IMAX=0
      DO 3 I=1,II
      IF(IRUN(I).GT.IMAX) IMAX=IRUN(I)
 3    CONTINUE
      OPEN(UNIT=50,FILE='TRSDAT.OUT',STATUS='UNKNOWN')
      WRITE(50,9) (I,I,I=1,5)
 9    FORMAT(2X,'RUN',5X,'DELAY',1X,5(2X,'I',I1,4X,'E',I1,1X))
      IDEL=0
      DO 5 III=IMIN,IMAX
      DO J=1,10
      SUMJ(J)=0.0
      ERRJ(J)=0.0
      END DO
      NFMAX=0
      DO 4 I=1,II
      IF(IRUN(I).NE.III) GO TO 4
      NF=IFRAM(I)
      IF(NF.GT.NFMAX) NFMAX=NF
      SUMJ(NF)=SUMI(I)
```

```
      ERRJ(NF)=ERRI(I)
 4    CONTINUE
      IF(NFMAX.NE.0) THEN
      IDEL=IDEL+1
      WRITE(50,6) III,DEL(IDEL),(SUMJ(K),ERRJ(K),K=1,NFMAX)
 6    FORMAT(2X,I5,3X,F6.3,5(2X,F5.1,1X,F3.1))
      END IF
 5    CONTINUE
      CLOSE(UNIT=50)
      STOP
      END
```

B.8 The TRAVER Program

```
      DIMENSION IRUN(5000),IFRAM(5000),SUMI(5000),ERRI(5000)
      DIMENSION SUMJ(256),ERRJ(256),npt(256)
      OPEN(UNIT=42,FILE='TRSTOR.DAT',STATUS='UNKNOWN')
      II=1
 99   CONTINUE
      READ(42,*,END=100) IRUN(II),IFRAM(II),SUMI(II),ERRI(II)
      II=II+1
      GO TO 99
 100  CONTINUE
      CLOSE(UNIT=42)
      II=II-1
      do 2 i=1,256
      npt(i)=0
      sumj(i)=0.0
      errj(i)=0.0
 2    continue
      imax=0
      do 1 i=1,ii
      if(ifram(i).gt.imax) imax=ifram(i)
      npt(ifram(i))=npt(ifram(i))+1
      sumj(ifram(i))=sumj(ifram(i))+sumi(i)
      errj(ifram(i))=sqrt(errj(ifram(i))**2+erri(i)**2)
 1    continue
      do 3 i=1,imax
      sumj(i)=sumj(i)/npt(i)
      errj(i)=errj(i)/npt(i)
 3    continue
      OPEN(UNIT=50,FILE='TRSPER.OUT',STATUS='UNKNOWN')
      WRITE(50,9)
 9    FORMAT(2X,'Output from superperiods runs')
      write(50,*) imax
      DO 5 III=1,imax
      WRITE(50,6) iii,sumj(iii),errj(iii)
```

```
  6     FORMAT(2X,I5,3X,f7.2,3x,f7.2)
  5     CONTINUE
        CLOSE(UNIT=50)
        STOP
        END
```

B.9 The Diagnostic Programmes

B.9.1 The REGRED Program

```
C   Example program of how to write and read to DAE registers using the SCSI
C interface.
C   This program has to be linked with a program call CLIENT_LINK.
C CLIENT_LINK contains the main program which controls the SCSI interface.  The
C main program calls the function called FORTRAN_PROGRAM, the soures code of
C which is in this file.
C
C   To compile and link (if program is called fortest):
C $ for fortest
C $ define dce horus$dka300:[sys12.syscommon.dce$library]
C $ define client_link axplib$disk:[ice2.v1_0c.vax]client_link
C $ link fortest,client_link/opt,dce:dce/opt
C

INTEGER FUNCTION FORTRAN_PROGRAM
IMPLICIT NONE

INCLUDE '($SYIDEF)'

C Declare function return values
INTEGER*4 SYS$TRNLOG
INTEGER*4 OPEN_DAE
INTEGER*4 CLOSE_DAE
INTEGER*4 WIO
INTEGER*4 RIO

C Delare variables
CHARACTER*15 INST_NAME
INTEGER*4 INST_LEN,IREG
c INTEGER*4 ADDRESS
c INTEGER*2 DATA,IVAL
INTEGER*4 DATA,IVAL
INTEGER*4 STATUS
INTEGER*2 IO_CHANNEL

C Before a any communictation is made to the DAE it has to be connected.
C The connection proocedure is as follows (with checks).
```

```
STATUS=SYS$TRNLOG('INST_NAME',INST_LEN,INST_NAME,,,)
IF (.NOT. STATUS) THEN
  TYPE *, 'SYS$TRNLOG failed'
  STOP
  ENDIF
STATUS = OPEN_DAE(INST_NAME(:INST_LEN))
IF (.NOT. STATUS) THEN
  TYPE *, 'OPEN_DAE failed'
  STOP
  ENDIF
IO_CHANNEL = 0
C DAE is now connected

C Talk to DAE
C Use functions WIO to write to DAE and RIO to read.
C paramiters: (INTEGER*4 address, INTEGER*2 data, INTEGER*4 io_channel)
C io_channel is not used for SCSI interface (was needed for QBus)
        write(*,1)
  1     format(/,5x,'Enter register number to read ',$)
        read(*,*) ireg
        if(ireg.eq.2164.OR.IREG.EQ.2166.OR.IREG.EQ.2168.
     &     OR.IREG.EQ.2170.or.ireg.eq.2172.or.ireg.eq.2174) then
  STATUS = RIO(IREG, DATA, IO_CHANNEL)
IF (.NOT. STATUS) THEN
        TYPE *, 'RIO failed ',IREG
        GO TO 2
        end if
TYPE *, IREG,' reads ', DATA
        ELSE
        WRITE(*,3) IREG
  3     FORMAT(/,5X,'UNKNOWN REGISTER VALUE ',I5)
        end if


C When communiction with thew DAE is done and before the proogram finishes the
C DAE should be disconnected using the CLOSE_DAE function.
  2     CONTINUE
FORTRAN_PROGRAM = CLOSE_DAE()
RETURN
END
```

B.9.2 The REGSET Program

```
C   Example program of how to write and read to DAE registers using the SCSI
C interface.
C   This program has to be linked with an program call CLIENT_LINK.
C CLIENT_LINK contains the main program which controls the SCSI interface.  The
```

```
C main program calls the function called FORTRAN_PROGRAM, the soures code of
C which is in this file.
C
C   To compile and link (if program is called fortest):
C $ for fortest
C $ define dce horus$dka300:[sys12.syscommon.dce$library]
C $ define client_link axplib$disk:[ice2.v1_0c.vax]client_link
C $ link fortest,client_link/opt,dce:dce/opt
C

INTEGER FUNCTION FORTRAN_PROGRAM
IMPLICIT NONE

INCLUDE '($SYIDEF)'

C Declare function return values
INTEGER*4 SYS$TRNLOG
INTEGER*4 OPEN_DAE
INTEGER*4 CLOSE_DAE
INTEGER*4 WIO
INTEGER*4 RIO

C Delare variables
CHARACTER*15 INST_NAME
INTEGER*4 INST_LEN,IREG
c INTEGER*4 ADDRESS
c INTEGER*2 DATA,IVAL
INTEGER*4 DATA,IVAL
INTEGER*4 STATUS
INTEGER*2 IO_CHANNEL

C Before a any communictation is made to the DAE it has to be connected.
C The connection proocedure is as follows (with checks).
STATUS=SYS$TRNLOG('INST_NAME',INST_LEN,INST_NAME,,,)
IF (.NOT. STATUS) THEN
  TYPE *, 'SYS$TRNLOG failed'
  STOP
  ENDIF
STATUS = OPEN_DAE(INST_NAME(:INST_LEN))
IF (.NOT. STATUS) THEN
  TYPE *, 'OPEN_DAE failed'
  STOP
  ENDIF
IO_CHANNEL = 0
C DAE is now connected

C Talk to DAE
```

```
C Use functions WIO to write to DAE and RIO to read.
C paramiters: (INTEGER*4 address, INTEGER*2 data, INTEGER*4 io_channel)
C io_channel is not used for SCSI interface (was needed for QBus)
        write(*,1)
  1     format(/,5x,'Enter register number and value ',$)
        read(*,*) ireg,ival
        if(ireg.eq.2164.OR.IREG.EQ.2166.OR.IREG.EQ.2168.
     &     OR.IREG.EQ.2174) then
  STATUS = WIO( IREG, ival, IO_CHANNEL)
IF (.NOT. STATUS) THEN
        TYPE *, 'WIO failed ',IREG
        GO TO 2
        END IF
  STATUS = RIO(IREG, DATA, IO_CHANNEL)
IF (.NOT. STATUS) THEN
        TYPE *, 'RIO failed ',IREG
        GO TO 2
        end if
TYPE *, IREG,' reads ', DATA
        ELSE
        WRITE(*,3) IREG
  3     FORMAT(/,5X,'UNKNOWN REGISTER VALUE ',I5)
        end if


C When communiction with thew DAE is done and before the proogram finishes the
C DAE should be disconnected using the CLOSE_DAE function.
  2     CONTINUE
FORTRAN_PROGRAM = CLOSE_DAE()
RETURN
END
```

B.9.3 The REGLINK Link Command

```
$ link 'p1',axplib$disk:[ice2.v1_0c.vax]client_link/opt,dce:dce/opt
```

Where the parameter p1 is either REGSET or REGRED.

References

[1] U. Steigenberger, G. Eckold and M. Hagen, *Time-resolved studies on a millisecond time scale by elastic neutron scattering: transient properties of the ferroelectric phase transition in Rb_2ZnCl_4*, Physica B **213**, 1012 (1995)

[2] S.J. Payne, *Critical scattering and time resolved neutron diffraction studies of phase transitions*, PhD Thesis, Keele University (1998)

[3] M.E. Hagen, *The PRISMA Operating Program Manual*, Rutherford Appleton Laboratory Report RAL-94-085 (1994)

[4] M.E. Hagen, *The PRISMA GENIE Data Analysis Programs*, Rutherford Appleton Laboratory Report RAL-94-086 (1994)