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MEASUREMENT OF DEVICE LIMITATIONS IN DIGITAL LOGIC DEVICES

by

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1. INTRODUCTION

Described here are a series of tests on digital logic devices. The tests are designed to measure the device limitations. The devices tested were from the 74 series of logic families.

Tests were conducted on five different devices, as they each have different input and output circuits. The devices chosen were:-

(1) 7404 A single input inverter.
(2) 7414 A single input Schmitt inverter.
(3) 74240 A single input 3 state output inverter.
(4) 7400 A two input NAND gate.
(5) 7474 A D type clocked latch with preset and clear.

These devices are representative of most devices in the 74 series of logic with regard to input and output circuit parameters.

The results of these tests show the differences between nominally identical devices from different manufacturers[1]. Also differences between different families (i.e. standard TTL, Schottky and low power Schottky) of the same device are shown.

From the measurement of input threshold levels, noise margins can be calculated. The rate test shows the absolute minimum input pulse widths which can be used when selecting the family of a particular device.

2. TEST PROCEDURE

The test procedure was broken down into several individual tests, which were designed to test specific functional operations, these were:-

(1) Transfer characteristics of single input devices; to show input thresholds and output drive levels. The devices used were, 7404 normal input, 7414 Schmitt input, and 74240 minimum Schmitt three state output. This test was repeated for each logic family (standard, Schottky and low powered Schottky) and each manufacturer

(Fairchild, Motorola, National semiconductor, Signetics, Texas).

(2) Transfer characteristics of a two input device; to check for cross talk. The device tested was a 7400 2 input NAND. This test was similar to test 1 except that it was repeated for two input conditions. 1. 'A' input was driven with 'B' input high, 2. 'A' input joined to 'B' input. These tests were repeated for each family and manufacturer.

(3) Threshold levels of a clocked device 7474; each input device; ('D', 'CLOCK', 'PRESET' and 'CLEAR') in turn was varied in amplitude until a change in state of the output occurred. These tests were repeated for each family and manufacturer.

(4) Rate characteristics of single input device 7404; as the input pulse was decreased in width until no change in state of the output occurs. These tests were repeated for each family and manufacturer.

(5) Rate characteristics of a clocked device, 7474; each input ('CLOCK' and 'CLEAR') in turn was driven by a decreasing width input pulse until no change in state of the output occurred. This series of tests was repeated for each family and manufacturer.

2.1 Test 1

The first test determined the output levels, threshold and hysteresis, of the 7404, 7414 and 74240 devices. A table for each device compares manufacturers and families.

With reference to fig.1 and fig.2, the device under test was inserted into the test jig and precisely 5 V was applied to the Vcc pin. The output of a sawtooth generator (H.P.8082A) was set to 5 V amplitude, 1.5 ms period, with rise and fall times of 500 µs (fig.7). This gave a clear slow transition suitable for display on an oscilloscope. This output drove both the device under test (d.u.t.) and the X axis of the oscilloscope. The output of the d.u.t was connected to the Y axis of the oscilloscope.

The oscilloscope displayed both the 'low' to 'high' and 'high' to 'low' output transitions. The difference being the hysteresis of the device. A multi-exposure photograph was taken of five devices of each type to show device spread. Typical photographs are shown in figs.8-13. Tables 1-3 show the 'low' level and 'high' level output voltages together with the threshold levels and hysteresis. The test was repeated for:-

(a) The different manufacturers

(b) The three families

(c) The devices 7404, 7414, 74240

(d) On full load (Vcc = 4.75, 5.00, 5.25 V)

(e) Off load (Vcc = 5.0 V only.)

2.2 Test 2

This test determined whether the level of the second input of a 7400 has any effect on the threshold level of the driven input.

Figure 3 shows the test jig used. The supply voltage was set to 5 V and full load applied (fig.6). This test is similar to test 1, except that the second input 'B', of the 7400 was tied 'high' for the first photographic exposure, then it was tied to input 'A' and the second exposure was taken. This was repeated for five devices of each type giving ten exposures of the photograph for each family to show device spread. The test was then repeated for:-

(a) The different manufacturers

(b) The three families.

2.3 Test 3

(a) This test determined the clock threshold and also checked if the level of 'D' had any effect.

Figure 4 shows the test jig used. A 7474 was placed in the test jig connected as in fig.5(a), with the 'D' input switched to 0 V. The supply was set to 5 V and full load applied. Pulses were driven into the 'clock' input with increasing amplitude from a pulse generator[2]. After each attempt to clock the latch the 'preset' input was driven 'low'. The minimum amplitude needed to reliably clock the 'D' signal to 'Q' was noted. The 'D' input was then switched to 5 V via a 1 kohm pull up resistor and the test was repeated. After each attempt to clock the latch the 'clear' input was driven 'low'. The minimum amplitude needed to reliably clock the 'D' signal to 'Q' was noted. Table 4 shows the minimum, average and maximum 'clock' thresholds needed to clock the latch for each sample from each manufacturer and both states of the 'D' input. The test was then repeated for:-

(a) The different manufacturers

(b) The three families.

(b) This test determined the 'preset' and 'clear' thresholds. A 7474 was placed in the test jig (fig.5(b)) with 'D' input and the 'clock' input connected to 5 V and full load applied. Pulses of increasing amplitude were fed into the 'clear' input. As this is a low active input, the pulse generator had its offset set to 3.5 V and gave negative going pulses of variable amplitude from a fixed offset. After each attempt to clear the latch the 'preset' input was driven 'low'. The minimum amplitude needed to reliably clear the 'Q' signal was noted. The circuit was rearranged to test the 'preset' input. Table 5 shows the minimum, average and maximum 'clear' and 'preset' thresholds. The test was then repeated for:-

(a) The different manufacturers

(b) The three families

(c) This test determined the 'D' input threshold of a 7474. Figure 5(c) shows the circuit used to measure the 'D' threshold. A 7474 was placed in the test jig with the 'D' input connected to a variable power supply. The supply rail was set to 5 V and full load applied. The latch was clocked from a pulse generator, after each attempt to clock the latch the 'clear' input was driven 'low'. The voltage on 'D' was increased until the 'D' threshold was reached. The minimum, average and maximum thresholds for each manufacturer were noted in Table 6. The test was then repeated for:-

(a) The different manufacturers

(b) The three families

2.4 Test 4

This test determined the minimum input pulse width of a 7404 for both 'low' and 'high' going pulses.

A 7404 was placed in the test jig (fig.1). The supply voltage was set to 5 V and full load was applied to the output. 2.0 V pulses with a D.C. offset of 0.5 V were supplied to the input of the circuit. This simulated the output of a fully loaded device. The pulse width was reduced and the output was monitored. The minimum width needed to reliably change states was noted (table 7), along with comments on the operation with even narrower pulses. The test was then repeated for:-

(a) The different manufacturers

(b) The three families

2.5 Test 5

(a) This test determined the minimum clock pulse widths of a 7474.

A 7474 was placed in the test jig with 'D' input connected to 0.5 V. The supply voltage was set to 5 V and full load was applied. Pulses of decreasing width were supplied to the 'clock' input. After each attempt to clock the latch, the 'present' input was driven 'low' to preset the output for the next attempted clock. The minimum width needed to reliably clear the 'Q' signal was noted (table 8), along with comments on the operation with even narrower pulses. The test was then repeated for:-

(a) The different manufacturers

(b) The three families

(b) This test determined the minimum 'clear' pulse needed for correct operation of a 7474.

A 7474 was placed in the test jig with 'D' input connected to 0.5 V. The supply voltage was set to 5 V and full load was applied. Pulses of decreasing width were supplied to the 'clear' input. After each attempt to clear the latch the preset input was driven 'low'. The minimum width required to reliably clear the 'Q' signal was noted in table 9, along with comments on the operation with even narrower pulse. The test was then repeated for:-

(a) The different manufacturers

(b) The three families

3. CONCLUSIONS

The definitions of TTL signals are:-

0 V	<	'low' input level	<	0.8 V
2.0 V	<	'high' input level	<	Vcc
0 V	<	'low' output level	<	0.6 V
2.4	<	'high' output level	<	Vcc
4.75 V	<	Vcc	<	5.25 V (+/- 5%)

For devices meeting these specifications the input threshold should be half way between 'low' and 'high' input levels. For best noise margins the correct threshold is then 1.4 V.

From table 1 it can be seen that the 'high' output level is much greater than the minimum allowable 'high' level, whereas the 'low' output level is close to the maximum allowable 'low' level. This giving a lower noise margin for 'low' signals.

The measured threshold level of a 7404 shows that it is referred to 0 V and independent of variations of both Vcc and load over the normal operating range. The main effect of variations in Vcc over the normal operating range is to change the high output level, therefore it will not contribute to noise in the system.

The effect of load on the output of the 7404 is to increase the 'low' level output voltage thus reducing the noise margin. This occurs irrespective of family.

Low power Schottky devices in general tend to have the lowest noise immunity with the exception of those manufactured by National Semiconductor and Signetics.

Table 2 shows the effect of a Schmitt input device 7414. Although the output levels vary much the same with Vcc and load, the noise margins are much greater due to the action of hysteresis. In general the larger the amount of hysteresis, the better the noise immunity. It can be seen that the threshold levels of the Schmitt devices vary with Vcc and

hysteresis increase with Vcc.

Table 3 shows that the amount of hysteresis of a 74240 decreases with load. The device has a linear positive going transfer function and a negative going transfer function with hysteresis (fig.13).

The results of test 2, on a two input device 7400 showed that the effect of the second input on the transfer characteristics was a less than 50 mV shift in threshold level in all cases, therefore crosstalk is unlikely to have significant effect.

Table 4 shows the results of test 3(a) on a 7474. Firstly it shows that the threshold level of the clock is independent of the level of the 'D' input. Secondly Motorola L.S. and Texas L.S. have low clock threshold levels and so will be less immune to noise than devices of other manufacturers.

The results of test 3(b) are shown in table 5. Both the 'preset' and 'clear' inputs have similar thresholds. Texas L.S. again has low thresholds, but as the 'preset' and 'clear' input are 'low' active the threshold level is probably of little consequence.

Table 6 shows the results of test 3(c). It can be seen that the 'D' input is within TTL threshold levels in all families by all manufacturers.

The minimum input pulse width of a 7404 (test 4) is shown in table 7. The minimum pulse width for an L.S. device is similar to the standard device, with 'S' device being between two and five times faster.

Table 8 gives the minimum clock pulse width of a 7474 for correct operation. Below this minimum width three conditions have been observed: 1. a double pulse on the output (fig.14), 2. a glitch on the output that recovers to the original state in 10-1000 ns (fig.15). 3. no operation, this is the most desirable condition. Signetics L.S. and Texas L.S. devices will operate with a considerably narrower clock than devices from other manufacturers. The 'S' device in general operates fastest.

Table 9 shows the 'clear' input to also have unstable conditions in response to narrow 'clear' signals. The 'S' device in general operates fastest.

Commonly noise problems in laboratory instruments are observed on transfer from earth plane prototypes to P.C.B's, due to lack of appreciation of the importance of an adequate earth plane.

5. TABLE CAPTIONS

1. Table of 7404 output levels and threshold level against supply variations and load.

2. Table of 7414 output levels, threshold levels and hysteresis against supply variation and load.

3. Table of 74240 output levels, threshold levels and hysteresis against supply variation and load.

4. Table of 7474 'clock' threshold levels against level of 'D'.

5. Table of 7474 'preset' and 'clear' thresholds.

6. Table of 7474 'D' threshold level.

7. Table of 7404 minimum pulse input width against 'high' and 'low' going input signals.

8. Table of 7474 minimum clock pulse width with comments on operation with narrower clock pulses.

9. Table of 7474 minimum preset and clear pulse width with comments on the operation with narrower input pulses.

TABLE 1 - DEVICE 7404

DEVICE	MANUFACTURER	VOLTS OUTPUT LOW LEVEL				VOLTS OUTPUT HIGH LEVEL				THESHOLD
		OFF LOAD	ON LOAD			OFF LOAD	ON LOAD			
		VCC VOLTS								
		5.0	4.75	5.0	5.25	5.0	4.75	5.0	5.25	
7404	FAIRCHILD	0.0	0.29	0.29	0.29	4.20	4.00	4.20	4.40	1.40
	NATIONAL	0.0	0.22	0.22	0.22	4.00	3.80	4.00	4.30	1.42
	SIGNETICS	0.0	0.30	0.30	0.30	4.00	3.80	4.00	4.30	1.41
	TEXAS	0.0	0.24	0.24	0.24	4.00	3.80	4.00	4.20	1.43
74LS04	FAIRCHILD	0.15	0.34	0.34	0.34	4.60	4.40	4.60	4.90	1.08
	MOTOROLA	0.12	0.33	0.33	0.33	4.20	4.00	4.20	4.40	1.04
	NATIONAL	0.12	0.38	0.38	0.38	4.30	4.00	4.30	4.50	1.40
	SIGNETICS	0.10	0.34	0.34	0.34	4.60	4.40	4.60	4.90	1.30
	TEXAS	0.20	0.46	0.46	0.48	4.40	4.10	4.40	4.60	1.10
74S04	FAIRCHILD	0.20	0.34	0.34	0.34	4.00	3.75	4.00	4.20	1.52
	NATIONAL	0.20	0.33	0.33	0.33	4.00	3.75	4.00	4.20	1.40
	SIGNETICS	0.25	0.43	0.43	0.43	4.00	3.75	4.00	4.20	1.30
	TEXAS	0.30	0.43	0.43	0.43	3.80	3.60	3.80	4.10	1.48

TABLE 2 - DEVICE 7414

DEVICE	MANUFACTURER	VOLTS OUTPUT LOW LEVEL				VOLTS OUTPUT HIGH LEVEL			
		OFF LOAD	ON LOAD			OFF LOAD	ON LOAD		
		VCC VOLTS							
		5.0	4.75	5.0	5.25	5.0	4.75	5.0	5.25
74LS14	FAIRCHILD	0.15	0.33	0.33	0.33	4.60	4.40	4.60	4.90
	MOTOROLA	0.15	0.31	0.31	0.31	4.60	4.40	4.60	4.90
	NATIONAL	0.20	0.38	0.38	0.38	4.30	4.00	4.30	4.50
	SIGNETICS	0.20	0.37	0.37	0.37	4.60	4.40	4.60	4.90
	TEXAS	0.20	0.39	0.39	0.39	4.60	4.40	4.60	4.90
7414	FAIRCHILD	0.0	0.29	0.29	0.29	4.10	3.80	4.00	4.20
	NATIONAL	0.0	0.20	0.20	0.20	4.20	3.90	4.10	4.40
	SIGNETICS	0.0	0.24	0.24	0.24	4.20	4.00	4.20	4.50
	TEXAS	0.0	0.26	0.26	0.26	4.10	3.90	4.10	4.40

DEVICE	MANUFACTURER	HIGH-LOW THESHOLD LEVEL			LOW-HIGH THESHOLD LEVEL			HYSTERESIS		
		VCC VOLTS			ON LOAD					
		4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25
74LS14	FAIRCHILD	0.96	1.00	1.04	1.70	1.76	1.86	0.74	0.76	0.82
	MOTOROLA	0.86	0.92	0.95	1.58	1.60	1.75	0.72	0.76	0.80
	NATIONAL	0.82	0.86	0.90	1.50	1.60	1.68	0.68	0.74	0.78
	SIGNETICS	0.87	0.90	0.96	1.64	1.72	1.79	0.77	0.82	0.83
	TEXAS	0.68	0.72	0.74	1.60	1.68	1.77	0.92	0.96	1.03
7474	FAIRCHILD	0.85	0.90	0.97	1.70	1.80	1.88	0.85	0.90	0.91
	NATIONAL	0.80	0.82	0.80	1.55	1.63	1.72	0.75	0.81	0.86
	SIGNETICS	0.87	0.96	1.04	1.72	1.81	1.92	0.89	0.85	0.88
	TEXAS	0.78	0.83	0.88	1.58	1.65	1.78	0.80	0.82	0.90

TABLE 3 - DEVICE 74240

DEVICE	MANUFACTURER	VOLTS OUTPUT LOW LEVEL				VOLTS OUTPUT HIGH LEVEL			
		OFF LOAD	ON LOAD			OFF LOAD	ON LOAD		
		VCC VOLTS							
		5.0	4.75	5.0	5.25	5.0	4.75	5.0	5.25
74LS240	FAIRCHILD	0.20	0.40	0.40	0.40	3.90	3.60	3.90	4.20
	MOTOROLA	0.10	0.31	0.31	0.31	3.80	3.60	3.80	4.10
	NATIONAL	0.15	0.37	0.37	0.37	3.90	3.60	3.90	4.10
	SIGNETICS	0.05	0.34	0.34	0.34	3.90	3.60	3.90	4.10
	TEXAS	0.10	0.34	0.34	0.34	3.80	3.50	3.80	4.00
74S240	NATIONAL	0.20	0.48	0.48	0.48	3.90	3.50	3.80	4.10
	TEXAS	0.20	0.44	0.44	0.44	3.90	3.60	3.90	4.20

DEVICE	MANUFACTURER	HIGH-LOW THESHOLD LEVEL		LOW-HIGH THESHOLD LEVEL		HYSTERESIS	
		LOAD					
		OFF	ON	OFF	ON	OFF	ON
74LS240	FAIRCHILD	1.00	1.10	1.55	1.55	0.55	0.45
	MOTOROLA	0.92	1.05	1.52	1.52	0.60	0.47
	NATIONAL	0.90	1.05	1.50	1.50	0.60	0.45
	SIGNETICS	1.02	1.15	1.45	1.45	0.43	0.30
	TEXAS	0.90	1.02	1.45	1.45	0.55	0.43
74S240	NATIONAL	1.21	1.32	1.60	1.60	0.39	0.28
	TEXAS	1.12	1.30	1.64	1.64	0.52	0.34

TABLE 4 - DEVICE 7474

DEVICE	MANUFACTURER	CLOCK THESHOLD LEVEL					
		`D' LOW			`D' HIGH		
		MIN	AVE	MAX	MIN	AVE	MAX
74LS74	FAIRCHILD	1.200	1.270	1.3000	1.260	1.270	1.290
	MOTOROLA	1.000	1.014	1.030	1.00	1.014	1.030
	NATIONAL	1.320	1.330	1.340	1.300	1.336	1.350
	SIGNETICS	1.240	1.340	1.440	1.230	1.286	1.440
	TEXAS	0.990	1.002	1.020	0.990	1.002	1.020
7474	FAIRCHILD	1.260	1.284	1.300	1.270	1.284	1.290
	NATIONAL	1.330	1.354	1.370	1.330	1.320	1.370
	SIGNETICS	1.290	1.318	1.360	1.290	1.336	1.370
	TEXAS	1.340	1.342	1.350	1.350	1.352	1.360
74S74	FAIRCHILD	1.280	1.308	1.320	1.260	1.290	1.310
	NATIONAL	1.230	1.274	1.230	1.240	1.285	1.320
	SIGNETICS	1.190	1.204	1.210	1.180	1.196	1.200
	TEXAS	1.280	1.298	1.320	1.290	1.304	1.320

TABLE 5 - DEVICE 7474

DEVICE	MANUFACTURER	CLEAR THESHOLD			PRESET THESHOLD		
		MIN	AVE	MAX	MIN	AVE	MAX
74LS74	FAIRCHILD	1.260	1.282	1.310	1.260	1.280	1.310
	MOTOROLA	1.390	1.404	1.420	1.300	1.404	1.420
	NATIONAL	1.290	1.320	1.330	1.310	1.330	1.340
	SIGNETICS	1.410	1.418	1.440	1.390	1.410	1.440
	TEXAS	0.920	0.946	0.990	0.920	0.948	0.990
7474	FAIRCHILD	1.320	1.340	1.360	1.360	1.370	1.390
	NATIONAL	1.390	1.394	1.410	1.390	1.394	1.400
	SIGNETICS	1.130	1.260	1.340	1.140	1.268	1.360
	TEXAS	1.360	1.362	1.370	1.360	1.362	1.380
74S74	FAIRCHILD	1.360	1.392	1.410	1.370	1.408	1.420
	NATIONAL	1.340	1.404	1.450	1.340	1.360	1.380
	SIGNETICS	1.250	1.278	1.290	1.250	1.270	1.280
	TEXAS	1.410	1.428	1.440	1.400	1.430	1.450

TABLE 6 - DEVICE 7474

DEVICE	MANUFACTURER	'D' THESHOLD LEVEL		
		MIN	AVE	MAX
74LS74	FAIRCHILD	1.200	1.212	1.240
	MOTOROLA	1.390	1.392	1.400
	NATIONAL	1.310	1.330	1.350
	SIGNETICS	1.160	1.160	1.160
	TEXAS	1.310	1.332	1.360
7474	FAIRCHILD	1.220	1.226	1.230
	NATIONAL	1.220	1.290	1.310
	SIGNETICS	1.240	1.268	1.300
	TEXAS	1.300	1.304	1.310
74S74	FAIRCHILD	1.250	1.278	1.290
	NATIONAL	1.190	1.236	1.270
	SIGNETICS	1.100	1.122	1.130
	TEXAS	1.260	1.270	1.290

TABLE 7 - DEVICE 7404

DEVICE	MANUFACTURER	MINIMUM INPUT PULSE WIDTH					
		LOW INPUT			HIGH INPUT		
		MIN	AVE	MAX	MIN	AVE	MAX
74LS04	FAIRCHILD	9.00	10.0	14.0	11.0	13.8	18.0
	MOTOROLA	9.00	10.2	11.0	16.0	18.2	20.0
	NATIONAL	8.00	8.80	9.00	7.00	7.00	7.00
	SIGNETICS	10.0	10.6	11.0	12.0	12.0	12.0
	TEXAS	11.0	11.6	13.0	13.0	14.4	16.0
7404	FAIRCHILD	12.0	13.6	16.0	13.0	15.4	19.0
	NATIONAL	11.0	11.2	12.0	11.0	12.0	13.0
	SIGNETICS	13.0	13.4	14.0	13.0	16.2	22.0
	TEXAS	10.0	10.8	13.0	11.0	11.8	15.0
74S04	FAIRCHILD	2.00	2.40	4.00	6.0	6.80	7.00
	NATIONAL	3.00	3.60	4.00	5.00	5.40	6.00
	SIGNETICS	2.00	2.00	2.00	6.00	6.00	6.00
	TEXAS	2.00	2.00	2.00	6.00	6.00	6.00

TABLE 8 - DEVICE 7474

DEVICE	MANUFACTURER	MINIMUM CLOCK PULSE WIDTH	RESPONSE TO NARROW CLOCK
74LS74	FAIRCHILD	10.0	GLITCHES LOW IN 60-100 NS RECOVERS IN 600-1000 NS
	MOTOROLA	12.0	<12.0 NS NO OPERATION
	NATIONAL	12.0	GLITCHES LOW RECOVERS IN 40 NS
	SIGNETICS	2.00	<2.00 NS NO OPERATION
	TEXAS	5.00	GLITCHES LOW RECOVERS IN 20 NS
7474	FAIRCHILD	12.0	8-10 NS DOUBLE PULSES,GLITCHES LOW FAST RECOVERY
	NATIONAL	16.0	14-16 NS DOUBLE PULSES,GLITCHES LOW 14 NS RECOVERY
	SIGNETICS	12.0	11-12 NS DOUBLE PULSES,<11 NS GLITCHES LOW
	TEXAS	19.0	17-19 NS DOUBLE PULSES,<17 NS GLITCHES LOW
74S74	FAIRCHILD	2.00	<2.00 NS NO OPERATION
	NATIONAL	2.00	<2.00 NS NO OPERATION
	SIGNETICS	4.00	GLITCHES LOW 30 NS RECOVERY
	TEXAS	3.00	GLITCHES LOW 15 NS RECOVERY

TABLE 9 - DEVICE 7474

DEVICE	MANUFACTURER	MINIMUM CLEAR PULSE WIDTH	RESPONSE TO NARROW CLEAR
74LS74	FAIRCHILD	5.00	GLITCHES LOW IN RECOVERS IN 600-1000 NS
	MOTOROLA	10.0	<10.0 NS NO OPERATION
	NATIONAL	3.00	GLITCHES LOW RECOVERS IN 20 NS
	SIGNETICS	5.00	<5.00 NS NO OPERATION
	TEXAS	3.00	<3.00 NS NO OPERATION
7474	FAIRCHILD	13.0	12-13 NS DOUBLE PULSES,10-12 NS GLITCHES FAST RECOVERY
	NATIONAL	14.0	13-14 NS DOUBLE PULSES,9-13 NS GLITCHES 60 NS RECOVERY
	SIGNETICS	14.0	12-14 NS DOUBLE PULSES,10-12 NS GLITCHES 40 NS RECOVERY
	TEXAS	18.0	15-18 NS DOUBLE PULSES,12-16 NS GLITCHES 50 NS RECOVERY
74S74	FAIRCHILD	3.00	2-3 NS GILTCH
	NATIONAL	2.00	<2.00 NS NO OPERATION
	SIGNETICS	3.00	2 NS GLITCHES LOW 10 NS RECOVERY
	TEXAS	2.00	<2.00 NS NO OPERATION

REFERENCES

1. Samples of five devices for each family, type and manufacturer were tested. Test results shown refer to this sample and other such samples may produce different results. Tests were conducted over a period where the temperature varied by no more than five degrees centigrade, thus the effect of temperature on the results will be insignificant.

2. The HP 8020A pulse generator was used in all tests.

FIGURE CAPTIONS

Fig.1 Test jig 1 for 7404, 7414 and 7474 devices used in tests 1,4. Wiring diagram for a 7404. Test configuration for test 1.

Fig.2 Test jig 2 for 74240 used in test 1. Wiring diagram for a 74240. Test configuration for test 1.

Fig.3 Test jig 3 for 7400 used in test 2. Wiring diagram for a 7400. Test configuration for test 2.

Fig.4 Test jig 4 for 7474 used in tests 3(a), 3(b), 3(b), 5(a), 5(a). Wiring diagram for a 7474.

Fig.5 Test configuration for test 3(a), 3(b), 3(c).

Fig.6 Load circuit. Table of maximum load against family and device.

Fig.7 Photograph of input signal.

Fig.8 Multi-exposure Photograph of 74LS04, all manufacturers.

Fig.9 Multi-exposure Photograph of 7404, all manufacturers.

Fig.10 Multi-exposure Photograph of 74S04, all manufacturers.

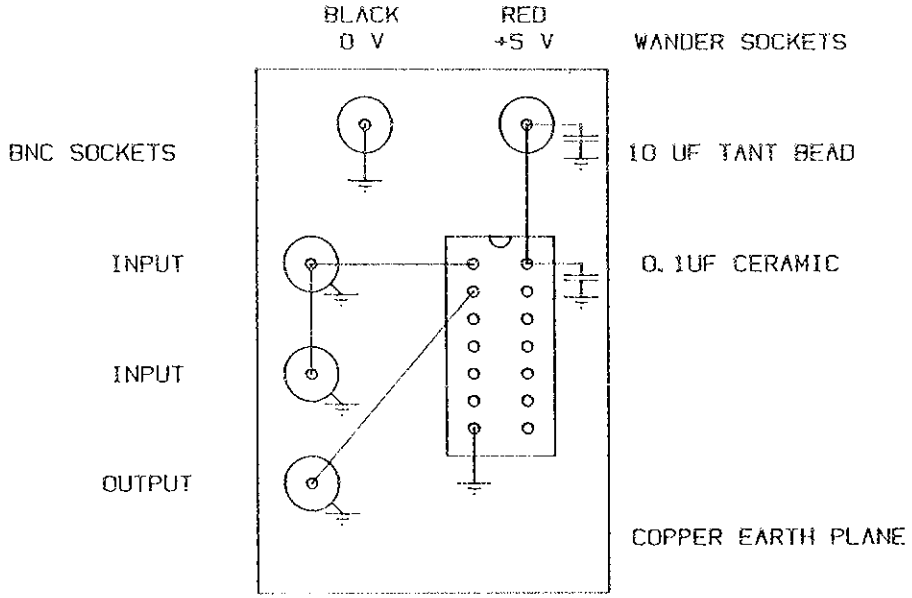
Fig.11 Multi-exposure Photograph of Fairchild 74LS04, 7404 and 74S04.

Fig.12 Multi-exposure Photograph of Texas 74LS04, 7404 and 74S04.

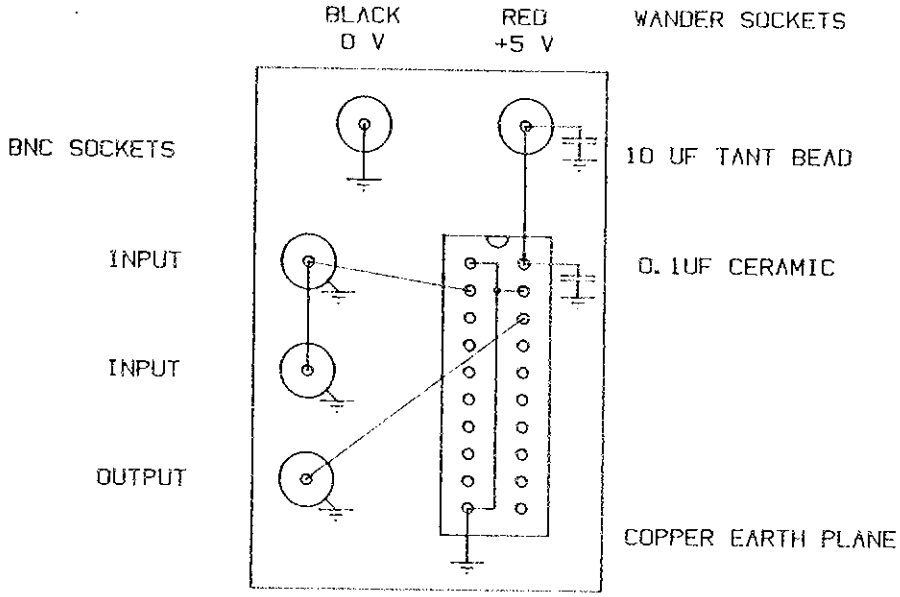
Fig.13 Multi-exposure Photograph of 74LS04 showing semi Schmitt transfer characteristic.

Fig.14 Photograph of 7474 in response to a narrow clock pulse. Double pulse output.

Fig.15 Photograph of 7474 in response to a narrow clock pulse. Glitch pulse output.



(a) JIG 1-14 PIN Z.I.F. SOCKET



(a) JIG 2-20 PIN Z.I.F. SOCKET

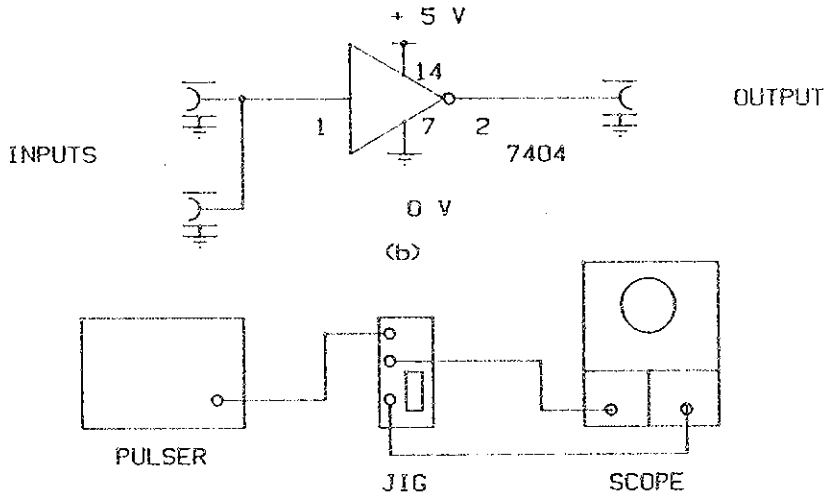


FIG. 1

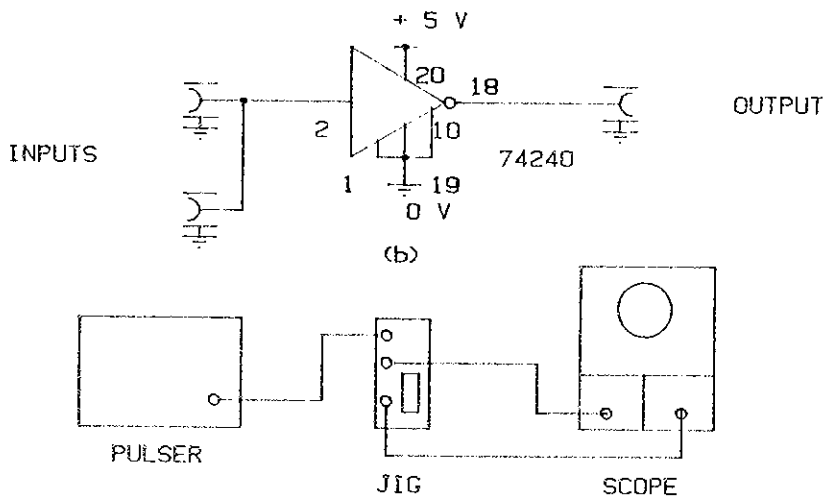
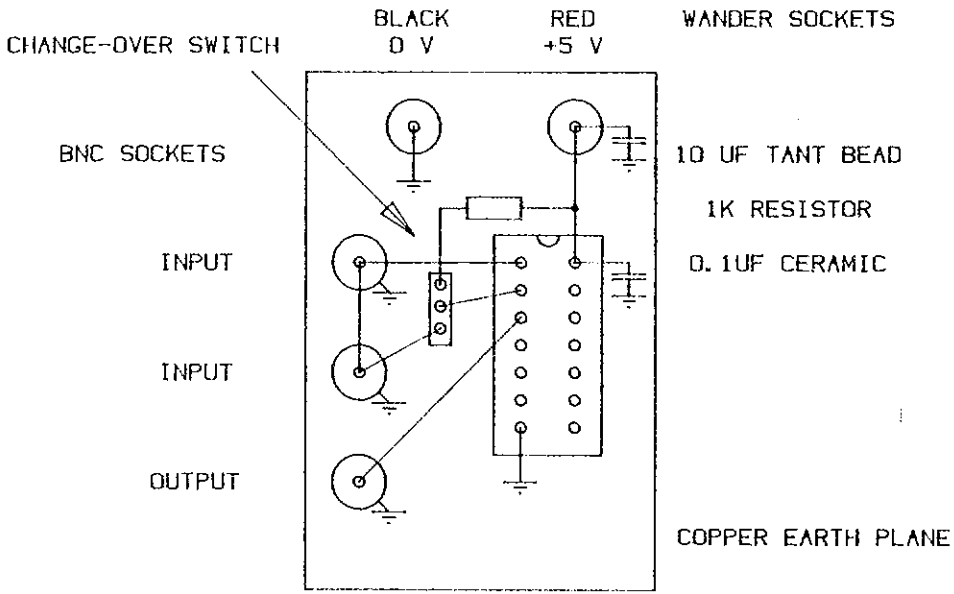
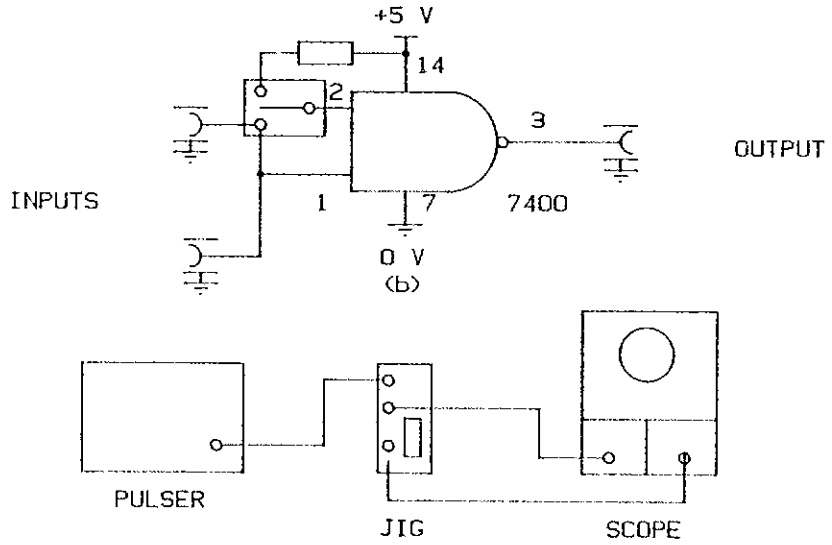


FIG. 2

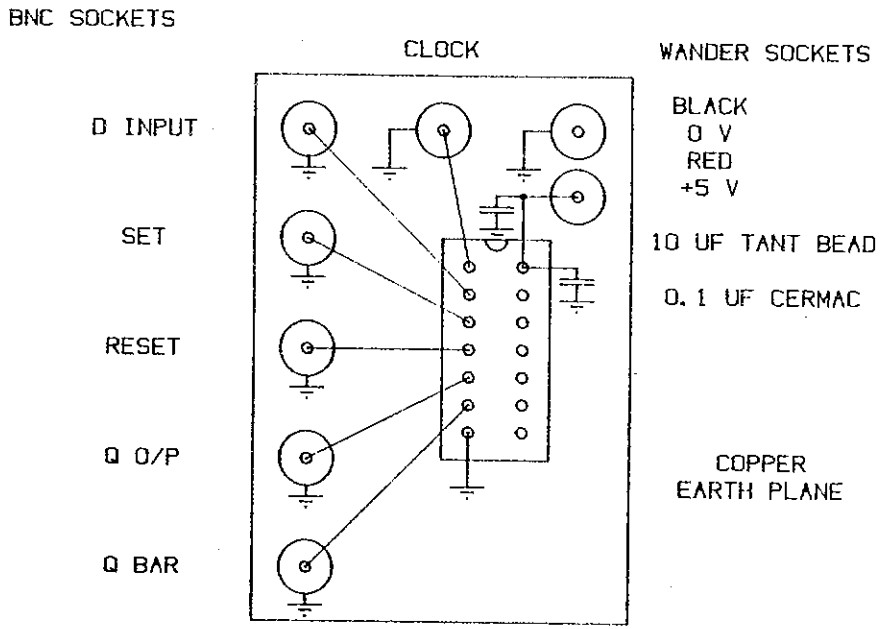


(a) JIG 3-14 PIN Z.I.F. SOCKET

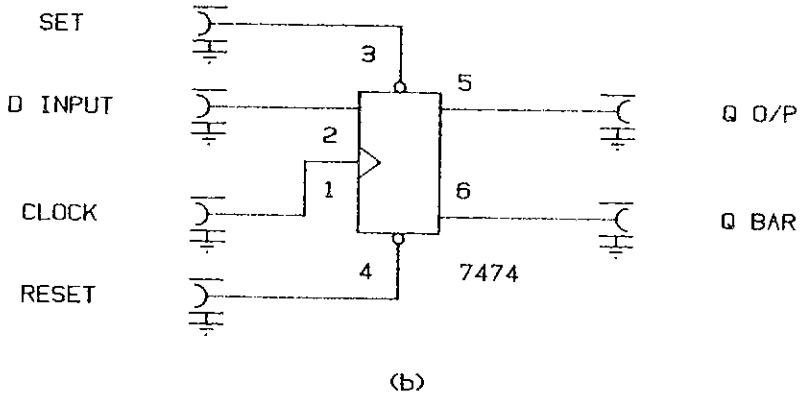


(c)

FIG. 3

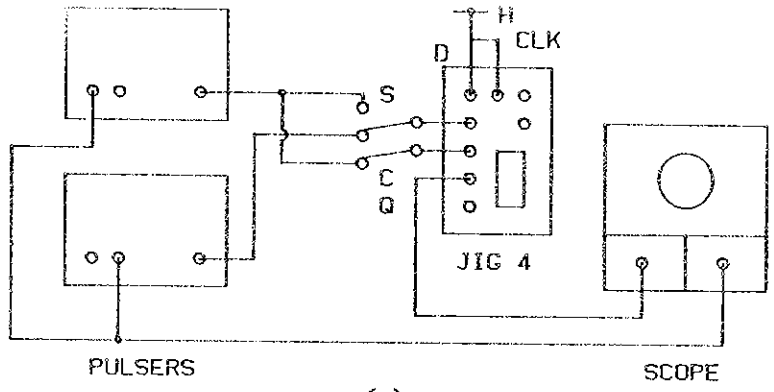


(a) JIG 4-14 PIN Z.I.F. SOCKET

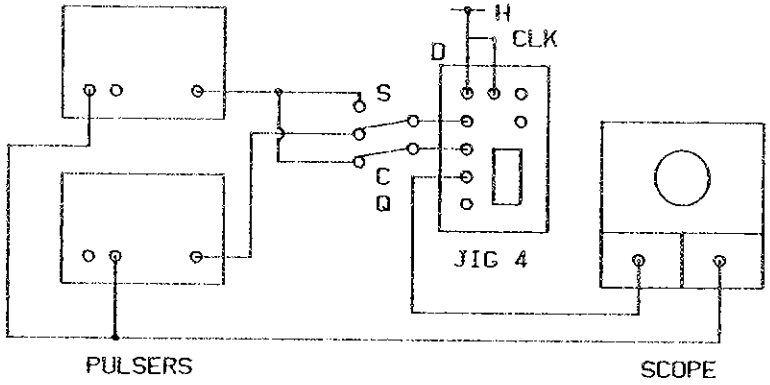


(b)

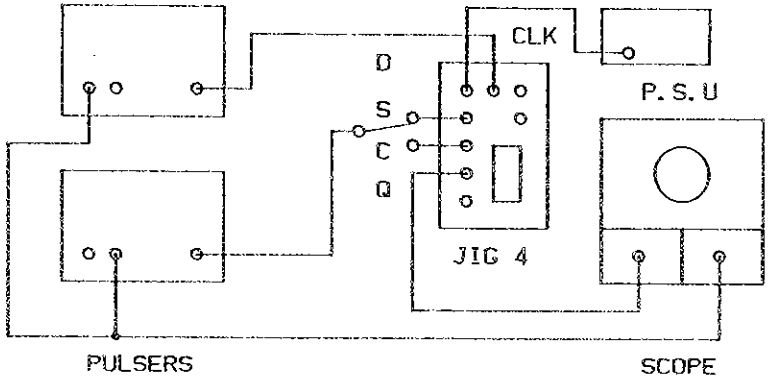
FIG. 4



(a)

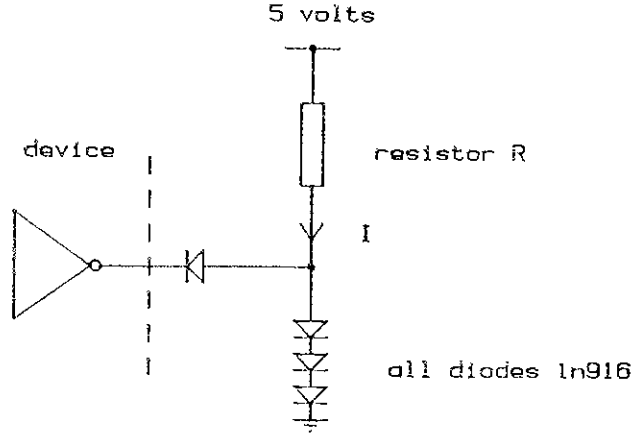


(b)



(c)

FIG. 5



device	family	resistance	current mA
7400	l.s	500	8
7404	std	250	16
7414	s.	200	20
7474			
74240	l.s.	160	24
	s.	62.5	64

FIG. 6

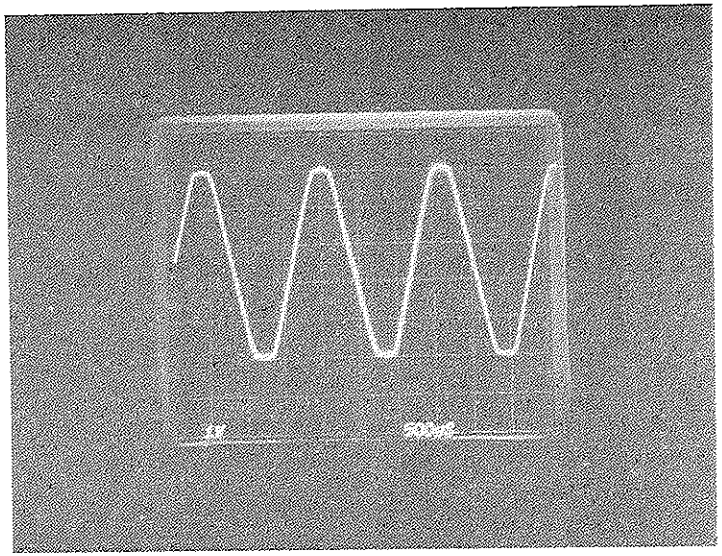


Fig. 7

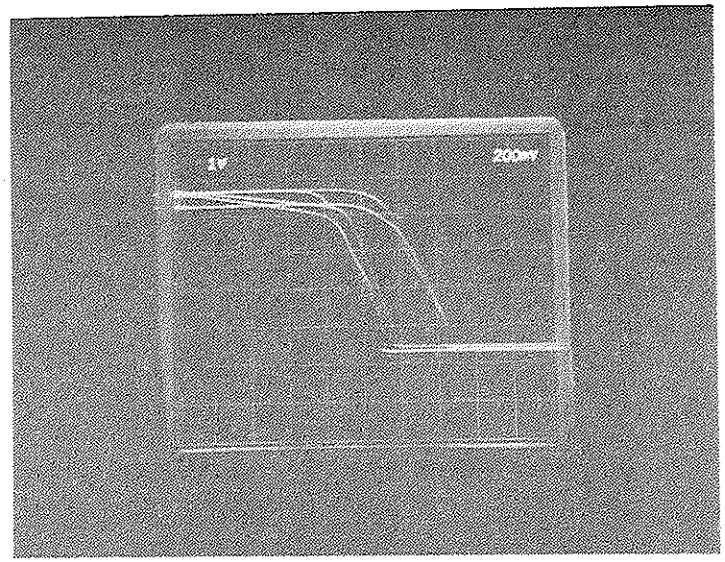


Fig. 8

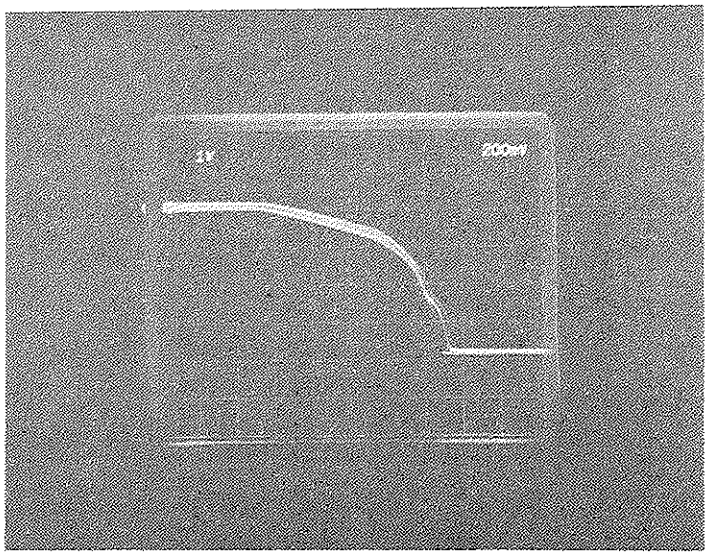


Fig. 9

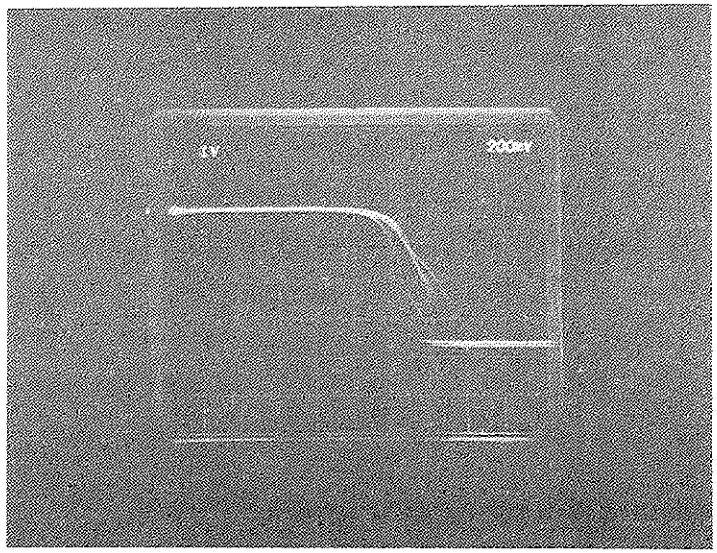


Fig. 10

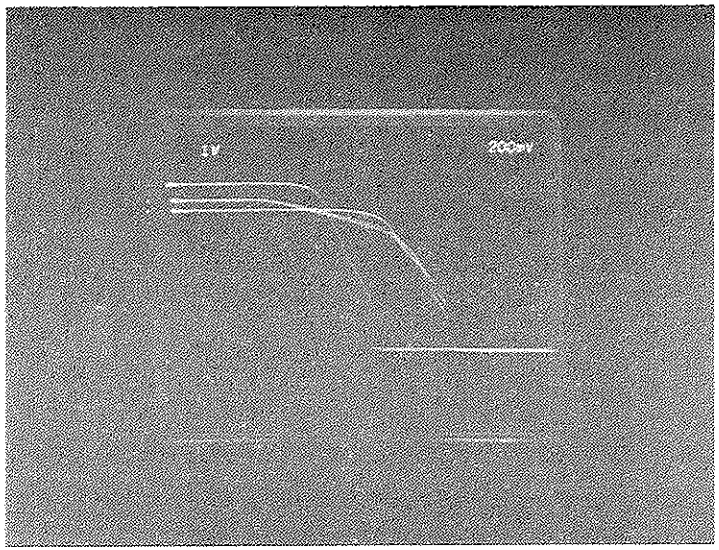


Fig.11

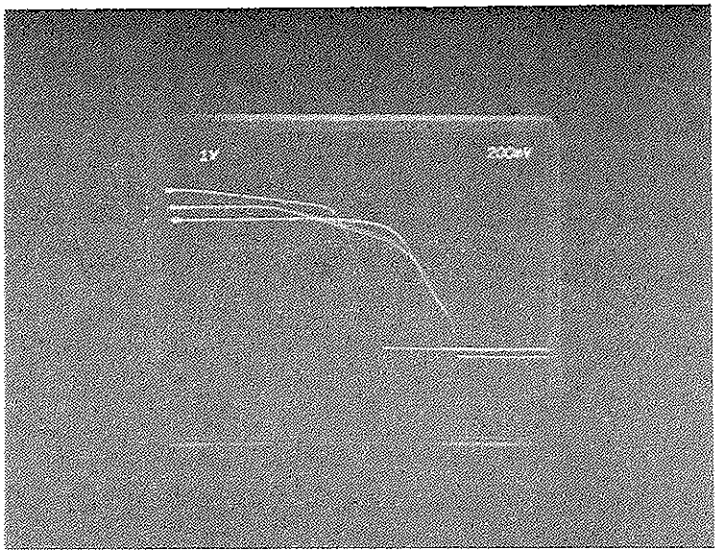


Fig.12

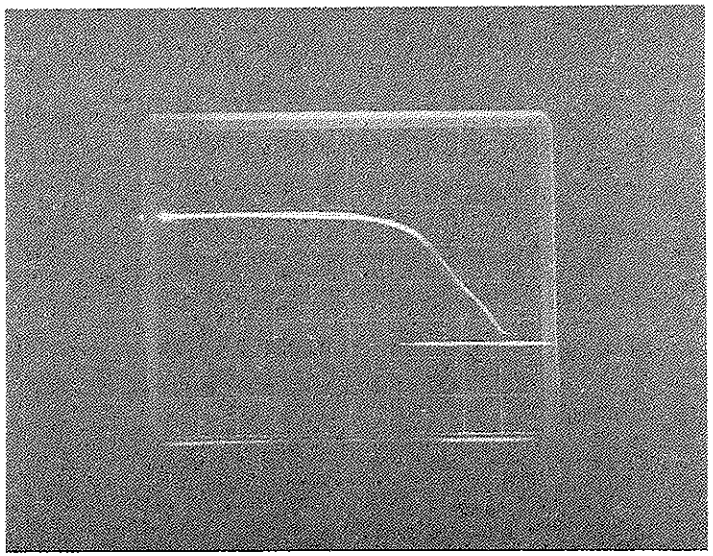


Fig.13

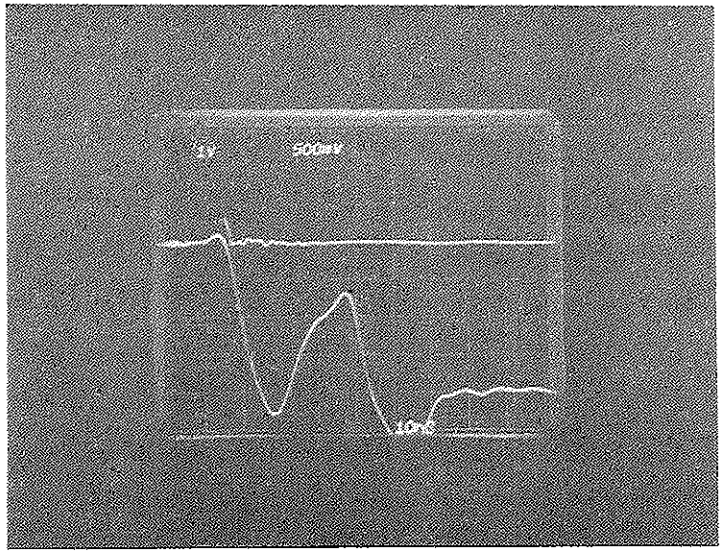


Fig.14

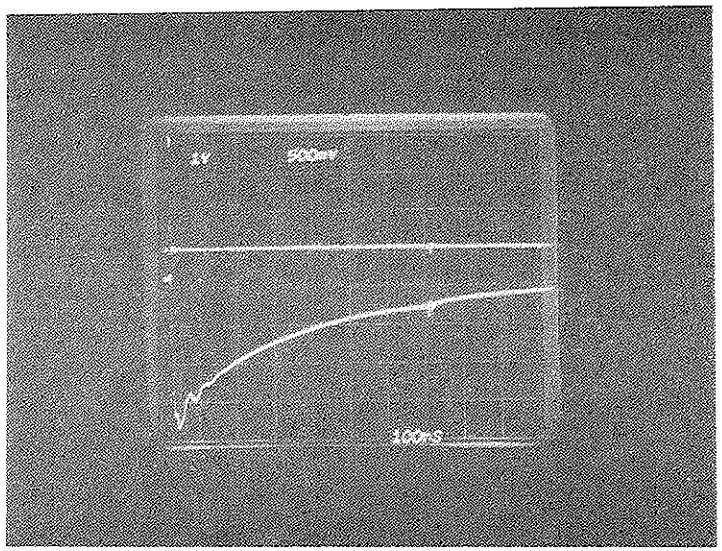


Fig.15