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INTERFACING CAMAC AUXILIARY CONTROLLERS TO THE DARESBURY MULTICRATE LINK SYSTEM

by

J. ALEXANDER, Daresbury Laboratory

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Science & Engineering Research Council

Daresbury Laboratory

Daresbury, Warrington WA4 4AD

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J. Alexander S.E.R.C. Daresbury Laboratory

1. INTRODUCTION

The Daresbury Multicrate Link System provides for several Camac Auxiliary Controllers (ACs) to control modules in seven Camac crates (or less) via a single inter-crate Link cable. The Link System philosophy and operation are described in reference 1. This document describes those features of an AC that are required to make use of the system.

2. SYSTEM DESCRIPTION

All Auxiliary Controllers using the Link System are situated in a single 'Master' crate containing the Link Driver module (EC529, or EC614: Link Driver with LAM Handler). They are connected to the Link Driver by an Auxiliary Controller Bus (ACB) cable at the rear of the crate, and by a Link Control Bus (LCB) cable at the front, as illustrated in figure 1. The Link Driver is connected to up to six Link Receiver modules (EC530, or EC615: Link Receiver with LAM Handler) in 'Slave' crates.

An AC's connection to, and use of, the ACB is exactly as defined in EUR6500 (reference 2). The additional features that an AC requires to make use of the Link System, and which are specified in this document, are:

1) A Link Control Bus (LCB) connector mounted on the front panel.

2) The ability to generate a 3-bit crate address.

3) A modified Camac timing sequence.

An AC also requires an interrupt intput if it is to use the optional LAM Handling feature of the Link System. This is a single pin LEMO connector, preferably mounted on the AC's front panel.

3. LCB CONNECTOR

The LCB connector is a '3M' style 20-pin header, type code 3428 or equivalent, mounted on the AC's front panel with pin 1 at top left when viewed from the front. It should preferably be mounted towards the top of the panel. The contact allocation is as follows:

Contact	Signal	Source
2	Start	AC
4	Continue	Link Driver
6	Strobe 1	AC
8	Strobe 2	AC
10	C1	AC
12	C2	AC
14	C4	AC
16,18,20	Reserved	
1,3,...,19	0 volts	AC and Link Driver

4. CRATE ADDRESS (C1, C2, C4)

The crate address is a 3-bit binary code that the AC places on the LCB to indicate which crate it wishes to access. The address of a crate is determined by the setting of a thumb-wheel switch mounted on the front panel of the Link Receiver or Link Driver installed in that crate. Note that address 0 is reserved for the optional LAM Handling feature, and that the Link Driver will automatically activate this feature whenever it detects an address of 0.

If the AC's sequence of operations is programmable (e.g. if it contains or is connected to a microprocessor), it is preferable that the crate address it generates for each Camac cycle can be specified by the program. It is also preferable that the crate address occupies the 3 most significant bits

of a byte whose other 5 bits specify the station address of a module within that crate. (N.B. The station address appears on the ACB as the Encoded-N signals described in reference 2.)

5. LCB ELECTRICAL SPECIFICATIONS

All signals on the LCB are 'low true' - i.e. a voltage of less than 0.8 volts represents a logic 1 and a voltage of greater than 2.0 volts represents a logic 0.

Signals generated on the LCB by an Auxiliary Controller must be driven with tri-state drivers. (Pull-up resistors for these signals are situated in the Link Driver.) The drivers must have the following characteristics:

Logic 1: When sinking 16 mA max. output voltage = 0.5 volts

Logic 0: When sourcing 2.6 mA min. output voltage = 2.4 volts

The CONTINUE signal is driven by the Link Driver with a standard totem-pole driver. Receivers in the ACs must have the following characteristics:

Logic 1: Input at 0.4 volts must source no more than 1.6 mA

Logic 0: Input at 3.5 volts must sink no more than 0.1 mA

Note that these specifications restrict the number of ACs that can use the Link System to 10. See reference 2 for other (more stringent) restrictions on the number of ACs that can be used in a single crate.

6. LCB SIGNAL TIMING

An AC may only assert signals on the LCB when it is asserting 'Request Inhibit' on the ACB. When it is not asserting Request Inhibit its LCB drivers must be in the high-impedance state.

Figure 2 shows the timing relationship between signals on the Camac dataway and the ACB and LCB. The timing reference points t0 to t9 are those defined in reference 3 (note that not all of them are identified in figure 2). All timing relationship specified in reference 3, as modified by reference 2, must be met. In addition:

tA The START signal must not be asserted at logic 1 until the 'command' signals (and dataway Write or 'W' signals if the command specifies a write operation) have been asserted. The 'command' signals are defined to be the dataway Busy, Function and Subaddress signals (B,F,A), together with the ACB Encoded-N signals (EN) and the LCB crate address signals (C4, C2 and C1).

t0 Upon receipt of the CONTINUE signal the pre-t3 delay of 500 nS minimum (as defined in reference 2) is started.

t3, t5, t6, t8 The Strobe-1 and Strobe-2 signals must be generated on the LCB at the same time as S1 and S2, respectively, on the dataway. The transitions of these signals must commence at the times indicated in reference 3, and complete no more than 20 nS later. This ensures that 'cleaner' versions of S1 and S2 than are available on the dataway are available for transmission to Slave crates.

t9 The START signal must remain asserted at logic 1 until t9. It should then be driven high to achieve minimum system delay.

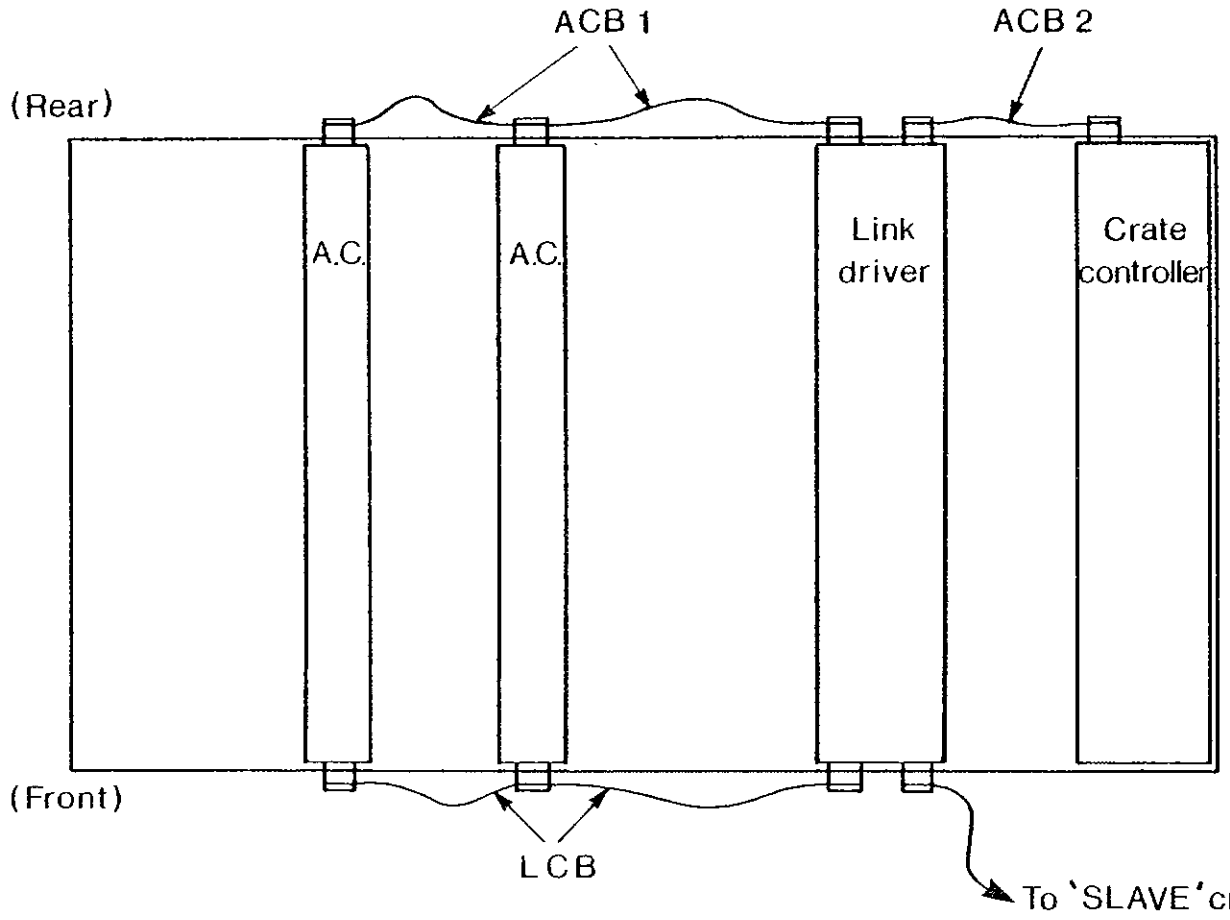
tB The Request Inhibit signal must not be released until the CONTINUE signal goes to logic 0. This is to ensure that the next AC to use the bus does not see CONTINUE still at 1 from the current cycle.

7. REFERENCES

1) 'A Multicrate Link System for use with Camac Auxiliary Controllers Designed at Daresbury Laboratory' by J. Alexander and J. Howson, Interfaces in Computing Vol. 1 page 171.

2) 'Multiple Controllers in a Camac Crate' CEC document EUR6500, and IEEE standard 675.

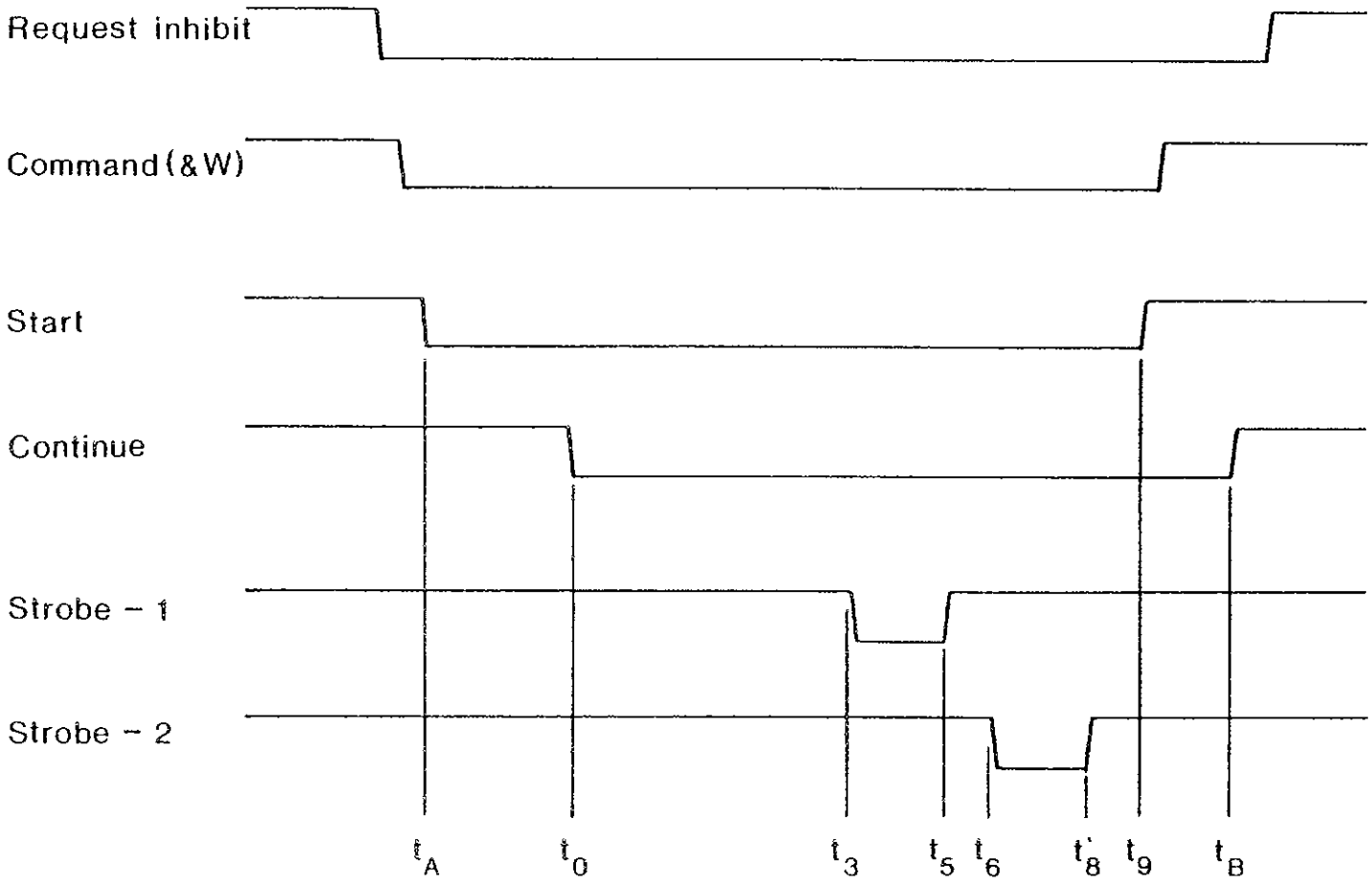
3) 'Camac - A Modular Instumentation System for Data Handling' CEC document EUR4100, and IEEE standard 583.



(N.B. Request / Grant-In / Grant-Out & Interrupt connections not shown)

PLAN VIEW OF 'MASTER' CRATE

Fig. 1


Request inhibit
Command (&W)
Start
Continue
Strobe – 1
Strobe – 2
t_A
t_0
t_3
t_5
t_6
t_8
t_9
t_B

TIMING

Fig.2